XC4000, XC4000A, XC4000H Logic Cell Array Families

Product Description

Features

- Third Generation Field-Programmable Gate Arrays
  - Abundant flip-flops
  - Flexible function generators
  - On-chip ultra-fast RAM
  - Dedicated high-speed carry-propagation circuit
  - Wide edge decoders
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution network
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and Interconnect
  - Low power consumption
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary-scan logic support
  - Programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per output (XC4000 family)
  - 24-mA sink current per output (XC4000A and XC4000H families)
- Configured by Loading Binary File
  - Unlimited reprogrammability
  - Six programming modes
- XACT Development System runs on '386/'486-type PC, NEC PC, Apollo, Sun-4, and Hewlett-Packard 700 series
  - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The XC4000 families of Field-Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array.

The XC4000 families provide a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs).

XC4000-family devices have generous routing resources to accommodate the most complex interconnect patterns. XC4000A devices have reduced sets of routing resources, sufficient for their smaller size. XC4000H high I/O devices maintain the same routing resources and CLB structure as the XC4000 family, while nearly doubling the available I/O.

The devices are customized by loading configuration data into the internal memory cells. The FPGA can either actively read its configuration data out of external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA (slave and peripheral modes).

The XC4000 families are supported by powerful and sophisticated software, covering every aspect of design: from schematic entry, to simulation, to automatic block placement and routing of interconnects, and finally the creation of the configuration bit stream.

Since Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening the design and development cycle, but they also offer a cost-effective solution for production rates well beyond 1000 systems per month.

Table 1. The XC4000 Families of Field-Programmable Gate Arrays

Device	XC4002A	4003/3A	4003H	4004A	4005/5A	4005H	4006	4008	4010/10D	4013/13D	4020	4025
Appr. Gate Count	2,000	3,000	3,000	4,000	5,000	5,000	6,000	8,000	10,000	13,000	20,000	25,000
CLB Matrix	8 x 8	10 x 10	10 x 10	12 x 12	14 x 14	14 x 14	16 x 16	18 x 18	20 x 20	24 x 24	28 x 28	32 x 32
Number of CLBs	64	100	100	144	196	196	256	324	400	576	784	1,024
Number of Flip-Flops	256	360	200	480	616	392	768	936	1,120	1,536	2,016	2,560
Max Decode Inputs (per side)	24	30	30	36	42	42	48	54	60	72	84	96
Max RAM Bits	2,048	3,200	3,200	4,608	6,272	6,272	8,192	10,368	12,800*	18,432*	25,088	32,768
Number of IOBs	64	80	160	96	112	192	128	144	160	192	224	256

*XC4010D and XC4013D have no RAM

XC4000 Compared to XC3000A

For those readers already familiar with the XC3000A family of Xilinx Field Programmable Gate Arrays, here is a concise list of the major new features in the XC4000 family.

CLB has two **independent** 4-input function generators.
A **third** function generator combines the outputs of the two other function generators with a ninth input.
All function inputs are swappable, all have full access; none are mutually exclusive.
CLB has **very fast arithmetic carry** capability.
CLB function generator look-up table can also be used as high-speed **RAM.**
CLB flip-flops have asynchronous set **or** reset.
CLB has **four outputs**, two flip-flops, two combinatorial.
CLB connections symmetrically located on all **four** edges.

IOB has more versatile clocking polarity options.
IOB has programmable input set-up time:
long to avoid potential hold time problems,
short to improve performance.
IOB has Longline access through its own TBUF.
Outputs are **n-channel only**, lower V_{OH} increases speed.
XC4000 outputs can be paired to double sink current to **24 mA.** XC4000A and XC4000H outputs can each sink 24 mA, can be paired for **48 mA** sink current.

IEEE 1149.1-type **boundary scan** is supported in the I/O.

Wide decoders on all four edges of the LCA device.

Increased **number of interconnect resources.**
All CLB inputs and outputs have **access to most interconnect lines.**
Switch Matrices are simplified to increase speed.
Eight global nets can be used for clocking or distributing logic signals.
TBUF output configuration is more versatile and 3-state control less confined.

Program is single-function input pin,overrides everything.
$\overline{\text{INIT}}$ pin also acts as Configuration Error output.

Peripheral Synchronous Mode (8 bit) has been added.
Peripheral Asynchronous Mode has improved handshake.
Start-up can be **synchronized** to any user clock (this is a configuration option).
No Powerdown, but instead a **Global 3-state input** that does not reset any flip-flops.
No on-chip **crystal oscillator** amplifier.

Configuration Bit Stream includes **CRC error checking.**
Configuration Clock can be increased to **>8 MHz.**
Configuration Clock is **fully static**, no constraint on the maximum Low time.

Readback either ignores flip-flop content (avoids need for masking) or it takes a **snapshot** of all flip-flops at the start of Readback.
Readback has same **polarity** as Configuration and can be **aborted.**

Table 2. Three Generations of Xilinx Field-Programmable Gate Array Families

Parameter	XC4025	XC3195A	XC2018
Number of flip-flops	2,560	1,320	174
Max number of user I/O	256	176	74
Max number of RAM bits	32,768	0	0
Function generators per CLB	3	2	2
Number of logic inputs per CLB	9	5	4
Number of logic outputs per CLB	4	2	2
Number of low-skew global nets	8	2	2
Dedicated decoders	yes	no	no
Fast carry logic	yes	no	no
Internal 3-state drivers	yes	yes	no
Output slew-rate control	yes	yes	no
Power-down option	no	yes	yes
Crystal oscillator circuit	no	yes	yes

Architectural Overview

The XC4000 families achieve high speed through advanced semiconductor technology and through improved architecture, and supports system clock rates of up to 50 MHz. Compared to older Xilinx FPGA families, the XC4000 families are more powerful, offering on-chip RAM and wide-input decoders. They are more versatile in their applications, and design cycles are faster due to a combination of increased routing resources and more sophisticated software. And last, but not least, they more than double the available complexity, up to the 20,000-gate level.

The XC4000 families have 16 members, ranging in complexity from 2,000 to 25,000 gates.

Logic Cell Array Families

Xilinx high-density user-programmable gate arrays include three major configurable elements: configurable logic blocks (CLBs), input/output blocks (IOBs), and interconnections. The CLBs provide the functional elements for constructing the user's logic. The IOBs provide the interface between the package pins and internal signal lines. The programmable interconnect resources provide routing paths to connect the inputs and outputs of the CLBs and IOBs onto the appropriate networks. Customized configuration is established by programming internal static memory cells that determine the logic functions and interconnections implemented in the LCA device.

The first generation of LCA devices, the XC2000 family, was introduced in 1985. It featured logic blocks consisting of a combinatorial function generator capable of implementing 4-input Boolean functions and a single storage element. The XC2000 family has two members ranging in complexity from 800 to 1500 gates.

In the second-generation XC3000A LCA devices, introduced in 1987, the logic block was expanded to implement wider Boolean functions and to incorporate a second flip-flop in each logic block. Today, the XC3000 devices range in complexity from 1,300 to 10,000 usable gates. They have a maximum guaranteed toggle frequency ranging from 70 to 270 MHz, equivalent to maximum system clock frequencies of up to 80 MHz.

The third generation of LCA devices further extends this architecture with a yet more powerful and flexible logic block. I/O block functions and interconnection options have also been enhanced with each successive generation, further extending the range of applications that can be implemented with an LCA device.

This third-generation architecture forms the basis of the XC4000 families of devices that feature logic densities up to 25,000 usable gates and support system clock rates of up to 50 MHz. The use of an advanced, sub-micron CMOS process technology as well as architectural improvements contribute to this increase in FPGA capabilities. However, achieving these high logic-density and performance levels also requires new and more powerful automated design tools. IC and software engineers collaborated during the definition of the third-generation LCA architecture to meet an important performance goal — an FPGA architecture and companion design tools for completely automatic placement and routing of 95% of all designs, plus a convenient way to complete the remaining few designs.

Configurable Logic Blocks

A number of architectural improvements contribute to the increased logic density and performance levels of the XC4000 families. The most important one is a more powerful and flexible CLB surrounded by a versatile set of routing resources, resulting in more "effective gates per CLB." The principal CLB elements are shown in Figure 1. Each new CLB also packs a pair of flip-flops and two independent 4-input function generators. The two function generators offer designers plenty of flexibility because most combinatorial logic functions need less than four inputs. Consequently, the design-software tools can deal with each function generator independently, thus improving cell usage.

Thirteen CLB inputs and four CLB outputs provide access to the function generators and flip-flops. More than double the number available in the XC3000 families, these inputs and outputs connect to the programmable interconnect resources outside the block. Four independent inputs are provided to each of two function generators (F1 – F4 and G1 – G4). These function generators, whose outputs are labeled F' and G', are each capable of implementing any arbitrarily defined Boolean function of their four inputs. The function generators are implemented as memory look-up tables; therefore, the propagation delay is independent of the function being implemented. A third function generator, labeled H', can implement any Boolean function of its three inputs: F' and G' and a third input from outside the block (H1). Signals from the function generators can exit the CLB on two outputs; F' or H' can be connected to the X output, and G' or H' can be connected to the Y output. Thus, a CLB can be used to implement any two independent functions of up-to-four variables, or any single function of five variables, or any function of four variables together with some functions of five variables , or it can implement even some functions of up to nine variables. Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased density and speed.

The two storage elements in the CLB are edge-triggered D-type flip-flops with common clock (K) and clock enable (EC) inputs. A third common input (S/R) can be programmed as either an asynchronous set or reset signal

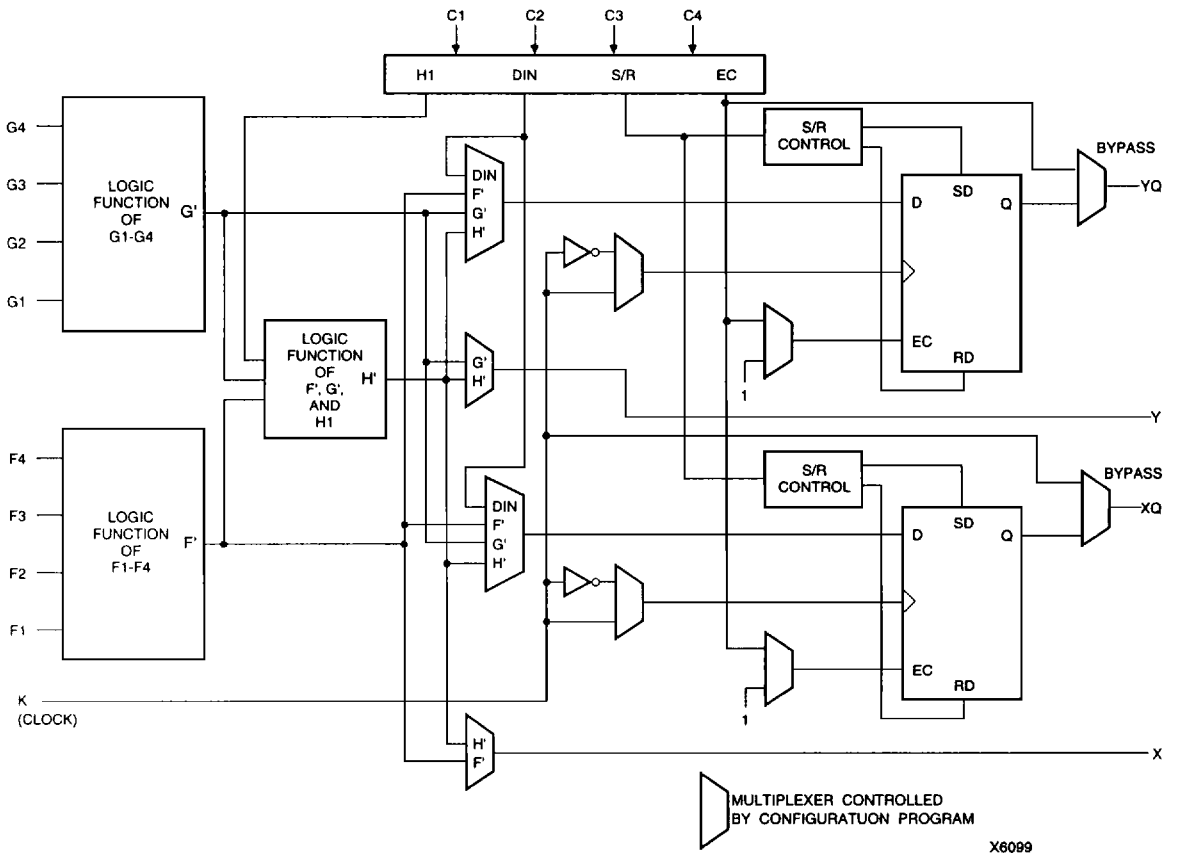


Figure 1. Simplified Block Diagram of XC4000-Families Configurable Logic Block

independently for each of the two registers; this input also can be disabled for either flip-flop. A separate global Set/Reset line (not shown in Figure 1) sets or clears each register during power-up, reconfiguration, or when a dedicated Reset net is driven active. This Reset net does not compete with other routing resources; it can be connected to any package pin as a global reset input.

Each flip-flop can be triggered on either the rising or falling clock edge. The source of a flip-flop data input is programmable: it is driven either by the functions F', G', and H', or the Direct In (DIN) block input . The flip-flops drive the XQ and YQ CLB outputs.

In addition, each CLB F' and G' function generator contains dedicated arithmetic logic for the fast generation of carry and borrow signals, greatly increasing the efficiency and performance of adders, subtracters, accumulators, comparators and even counters.

Multiplexers in the CLB map the four control inputs, labeled C1 through C4 in Figure 1, into the four internal control signals (H1, DIN, S/R, and EC) in any arbitrary manner.

The flexibility and symmetry of the CLB architecture facilitates the placement and routing of a given application. Since the function generators and flip-flops have independent inputs and outputs, each can be treated as a separate entity during placement to achieve high packing density. Inputs, outputs, and the functions themselves can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation.

Speed Is Enhanced Two Ways

Delays in LCA-based designs are layout dependent. While this makes it hard to predict a worst-case guaranteed performance, there is a rule of thumb designers can consider — the system clock rate should not exceed one third to one half of the specified toggle rate. Critical portions of a design, shift registers and simple counters, can run faster — approximately two thirds of the specified toggle rate.

The XC4000 family can run at synchronous system clock rates of up to 60 MHz. This increase in performance over the previous families stems from two basic improvements: improved architecture and more abundant routing resources.

Improved Architecture

More Inputs: The versatility of the CLB function generators improves system speed significantly. Table 3 shows how the XC4000 families implement many functions more efficiently and faster than is possible with XC3000 devices. A 9-bit parity checker, for example, can be implemented in one CLB with a propagation delay of 7 ns. Using a XC3000-family device, the same function requires two CLBs with a propagation delay of 2 x 5.5 ns = 11 ns. One XC4000 CLB can determine whether two 4-bit words are identical, again with a 7-ns propagation delay. The ninth input can be used for simple ripple expansion of this identity comparator (25.5 ns over 16 bits, 51.5 ns over 32 bits), or a 2-layer identity comparator can generate the result of a 32-bit comparison in 15 ns, at the cost of a single extra CLB. Simpler functions like multiplexers also benefit from the greater flexibility of the XC4000-families CLB. A 16-input multiplexer uses 5 CLBs and has a delay of only 13.5 ns.

More Outputs: The CLB can pass the combinatorial output(s) to the interconnect network, but can also store the combinatorial result(s) or other incoming data in one or two flip-flops, and connect their outputs to the interconnect network as well. With XC3000-families CLBs the designer has to make a choice, either output the combinatorial function or the stored value. In the XC4000 families, the flip flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated task. This increases the functional density of the devices.

When a function generator drives a flip-flop in a CLB, the combinatorial propagation delay *overlaps completely* with the set-up time of the flip-flop. The set-up time is specified between the function generator inputs and the clock input. This represents a performance advantage over competing technologies where combinatorial delays must be added to the flip-flop set-up time.

Fast Carry: As described earlier, each CLB includes high-speed carry logic that can be activated by configuration. The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level.

A 16-bit adder requires nine CLBs and has a combinatorial carry delay of 20.5 ns. Compare that to the 30 CLBs and 50 ns, or 41 CLBs and 30 ns in the XC3000 family.

The fast-carry logic opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast and/or not efficient enough. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

Faster and More Efficient Counters: The XC4000-families fast-carry logic puts two counter bits into each CLB and runs them at a clock rate of up to 42 MHz for 16 bits, whether the counters are loadable or not. For a 16-bit

Table 3. Density and Performance for Several Common Circuit Functions

		XC3000 (-125)		XC4000 (-5)	
16-bit Decoder From Input Pad		15 ns	4 CLBs	12 ns	0 CLBs
24-bit Accumulator		17 MHz	46 CLBs	32 MHz	13 CLBs
State Machine Benchmark*		18 MHz	34 CLBs	30 MHz	26 CLBs
16:1 Multiplexer		16 ns	8 CLBs	16 ns	5 CLBs
16-bit Unidirectional	Max Density	20 MHz	16 CLBs	40 MHz	8 CLBs
Loadable Counter	Max Speed	34 MHz	23 CLBs	42 MHz	9 CLBs
16-bit U/D Counter	Max Density	20 MHz	16 CLBs	40 MHz	8 CLBs
	Max Speed	30 MHz	27 CLBs	40 MHz	8 CLBs
16-bit Adder	Max Density	50 ns	30 CLBs	20.5 ns	9 CLBs
	Max Speed	30 ns	41 CLBs	20.5 ns	9 CLBs

* 16 states, 40 transitions, 10 inputs, 8 outputs

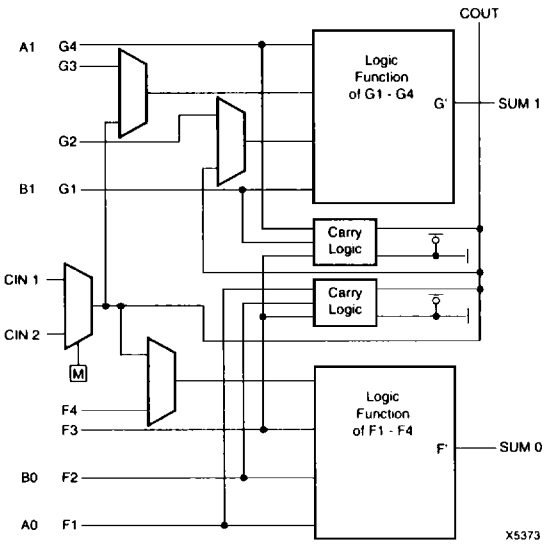


Figure 2. Fast Carry Logic in Each CLB

up/down counter, this means twice the speed in half the number of CLBs, compared with the XC3000 families.

Pipelining Speeds Up The System: The abundance of flip-flops in the CLBs invites pipelined designs. This is a powerful way of increasing performance by breaking the function into smaller subfunctions and executing them in parallel, passing on the results through pipeline flip-flops. This method should be seriously considered wherever total performance is more important than simple through-delay.

Wide Edge Decoding: For years, FPGAs have suffered from the lack of wide decoding circuitry. When the address or data field is wider than the function generator inputs (five bits in the XC3000 families), FPGAs need multi-level decoding and are thus slower than PALs. The XC4000-family CLBs have nine inputs; any decoder of up to nine inputs is, therefore, compact and fast. But, there is also a need for much wider decoders, especially for address decoding in large microprocessor systems. The XC4000 family has four programmable decoders located on each edge of each device. Each of these wired-AND gates is capable of accepting up to 42 inputs on the XC4005 and 72 on the XC4013. These decoders may also be split in two when a large number of narrower decoders are required for a maximum of 32 per device. These dedicated decoders accept I/O signals and internal signals as inputs and generate a decoded internal signal in 18 ns, pin-to-pin. The XC4000A family has only two decoder AND gates per edge which, when split provide a maximum of 16 per device. Very large PALs can be emulated by ORing the decoder outputs in a CLB. This decoding feature covers what has long been considered a weakness of FPGAs. Users often resorted to external PALs for simple but fast decoding functions. Now, the dedicated decoders in the XC4000 can implement these functions efficiently and fast.

Higher Output Current: The 4-mA maximum output current specification of today's FPGAs often forces the user to add external buffers, cumbersome especially on bidirectional I/O lines. The XC4000 families solve many of these problems by increasing the maximum output sink current to 12 mA. Two adjacent outputs may be interconnected to increase the output sink current to 24 mA. The FPGA can thus drive short buses on a pc board. The XC4000A and XC4000H outputs can sink 24 mA per output and can double up for 48 mA.

While the XC2000 and XC3000 families used complementary output transistors, the XC4000 outputs are n-channel for both pull-down and pull-up, somewhat analogous to the classical totem pole used in TTL. The reduced output High level (VOH) makes circuit delays more symmetrical for TTL-threshold systems. The XC4000H outputs have an optional p-channel output transistor.

Abundant Routing Resources

Connections between blocks are made by metal lines with programmable switching points and switching matrices. Compared to the previous LCA families, these routing resources have been increased dramatically.The number of globally distributed signals has been increased from two to eight, and these lines have access to any clock or logic input. The designer of synchronous systems can now distribute not only several clocks, but also control signals, all over the chip, without having to worry about any skew.

There are more than twice as many horizontal and vertical Longlines that can carry signals across the length or width of the chip with minimal delay and negligible skew.The horizontal Longlines can be driven by 3-state buffers, and can thus be used as unidirectional or bidirectional data buses; or they can implement wide multiplexers or wired-AND functions.

Single-length lines connect the switching matrices that are located at every intersection of a row and a column of CLBs. These lines provide the greatest interconnect flexibility, but cause a delay whenever they go through a switching matrix. Double-length lines bypass every other matrix, and provide faster signal routing over intermediate distances.

Compared to the XC3000 family, the XC4000 families have more than double the routing resources, and they are arranged in a far more regular fashion. In older devices,

inputs could not be driven by all adjacent routing lines. In the XC4000 families, these constraints have been largely eliminated. This makes it easier for the software to complete the routing of complex interconnect patterns.

Chip architects and software designers worked closely together to achieve a solution that is not only inherently powerful, but also easy to utilize by the software-driven design tools for Partitioning, Placement and Routing. The goal was to provide automated push-button software tools that complete almost all designs, even large and dense ones, automatically, without operator assistance. But these tools will still give the designer the option to get involved in the partitioning, placement and, to a lesser extent, even the routing of critical parts of the design, if that is needed to optimize the performance.

On-Chip Memory

The XC4000, XC4000A and XC4000H family devices are the first programmable logic devices with RAM accessible to the user.

An optional mode for each CLB makes the memory look-up tables in the F' and G' function generators usable as either a 16 x 2 or 32 x 1 bit array of Read/Write memory cells (Figure 3). The F1-F4 and G1-G4 inputs to the function generators act as address lines, selecting a particular memory cell in each look-up table. The functionality of the CLB control signals change in this configuration; the H1, DIN, and S/R lines become the two data inputs and the Write Enable (WE) input for the 16 x 2 memory. When the 32 x 1 configuration is selected, D1 acts as the fifth address bit and D0 is the data input. The contents of the memory cell(s) being addressed are available at the F' and G' function-generator outputs, and can exit the CLB through its X and Y outputs, or can be pipelined using the CLB flip-flop(s).

Configuring the CLB function generators as Read/Write memory does not affect the functionality of the other portions of the CLB, with the exception of the redefinition of the control signals. The H' function generator can be used to implement Boolean functions of F', G', and D1, and the D flip-flops can latch the F', G', H', or D0 signals.

The RAMs are very fast; read access is the same as logic delay, about 5.5 ns; write time is about 8 ns; both are several times faster than any off-chip solution. Such distributed RAM is a novel concept, creating new possibilities in system design: registered arrays of multiple accumulators, status registers, index registers, DMA counters, distributed shift registers, LIFO stacks, and FIFO buffers. The data path of a 16-byte FIFO uses four CLBs for storage, and six CLBs for address counting and multiplexing (Figure 4). With 32 storage locations per CLB, compared to two flip-flops per CLB, the cost of intelligent distributed memory has been reduced by a factor of 16.

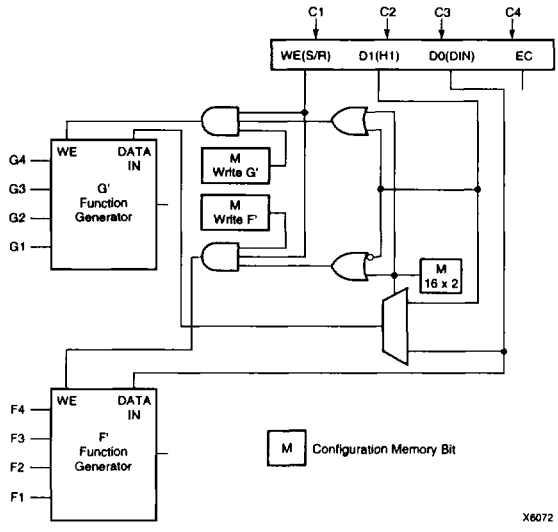


Figure 3. CLB Function Generators Can Be Used as Read/Write Memory Cells

Input/Output Blocks (IOBs), XC4000 and XC4000A Families

(for XC4000H family, see page 2-82)

User-configurable IOBs provide the interface between external package pins and the internal logic (Figure 5). Each IOB controls one package pin and can be defined for input, output, or bidirectional signals.

Two paths, labeled I1 and I2, bring input signals into the array. Inputs are routed to an input register that can be programmed as either an edge-triggered flip-flop or a level-sensitive transparent latch. Optionally, the data input to the register can be delayed by several nanoseconds to compensate for the delay on the clock signal, that first must

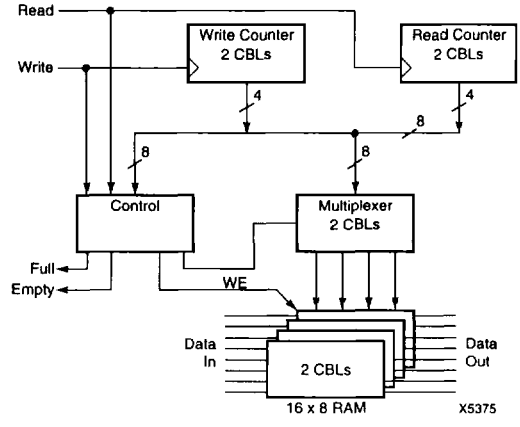


Figure 4. 16-byte FIFO

pass through a global buffer before arriving at the IOB. This eliminates the possibility of a data hold-time requirement at the external pin. The I1 and I2 signals that exit the block can each carry either the direct or registered input signal.

Output signals can be inverted or not inverted, and can pass directly to the pad or be stored in an edge-triggered flip-flop. Optionally, an output enable signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output enable (OE) signals can be inverted, and the slew rate of the output buffer can be reduced to minimize power bus transients when switching non-critical signals. Each XC4000-families output buffer is capable of sinking 12 mA; two adjacent output buffers can be wire-ANDed externally to sink up to 24 mA. In the XC4000A and XC4000H families, each output buffer can sink 24 mA.

There are a number of other programmable options in the IOB. Programmable pull-up and pull-down resistors are useful for tying unused pins to V_{CC} or ground to minimize power consumption. Separate clock signals are provided for the input and output registers; these clocks can be inverted, generating either falling-edge or rising-edge triggered flip-flops. As is the case with the CLB registers, a global set/reset signal can be used to set or clear the input and output registers whenever the RESET net is active.

Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary-scan testing, permitting easy chip and board-level testing.

Programmable Interconnect

All internal connections are composed of metal segments with programmable switching points to implement the desired routing. An abundance of different routing resources is provided to achieve efficient automated routing. The number of routing channels is scaled to the size of the array; i.e., it increases with array size.

In previous generations of LCAs, the logic-block inputs were located on the top, left, and bottom of the block; outputs exited the block on the right, favoring left-to-right data flow through the device. For the third-generation family, the CLB inputs and outputs are distributed on all four sides of the block, providing additional routing flexibility (Figure 6). In general, the entire architecture is more symmetrical and regular than that of earlier generations, and is more suited to well-established placement and routing algorithms developed for conventional mask-programmed gate-array design.

There are three main types of interconnect, distinguished by the relative length of their segments: single-length lines, double-length lines, and Longlines. Note: The number of routing channels shown in Figures 6 and 9 are for illustration purposes only; the actual number of routing channels varies with array size. The routing scheme was designed for minimum resistance and capacitance of the average routing path, resulting in significant performance improvements.

The single-length lines are a grid of horizontal and vertical lines that intersect at a Switch Matrix between each block. Figure 6 illustrates the single-length interconnect lines

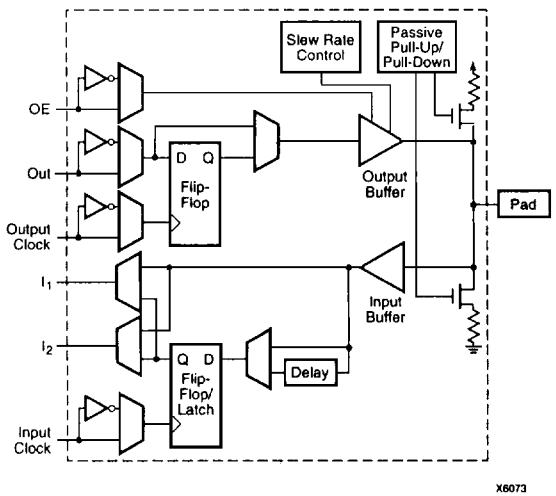


Figure 5. XC4000 and XC4000A Families Input/Output Block

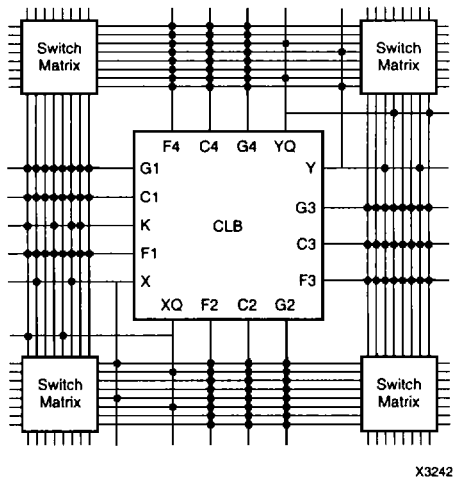


Figure 6. Typical CLB Connections to Adjacent Single-Length Lines

surrounding one CLB in the array. Each Switch Matrix consists of programmable n-channel pass transistors used to establish connections between the single-length lines (Figure 7). For example, a signal entering on the right side of the Switch Matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Single-length lines are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

Compared to the previous generations of LCA architectures, the number of possible connections through the Switch Matrix has been reduced. This decreases capacitive loading and minimizes routing delays, thus increasing performance. However, a much more versatile set of connections between the single-length lines and the CLB inputs and outputs more than compensate for the reduction in Switch Matrix options, resulting in overall increased routability.

The function generator and control inputs to the CLB (F1-F4, G1-G4, and C1-C4) can be driven from any adjacent single-length line segment (Figure 6). The CLB clock (K) input can be driven from one-half of the adjacent single-length lines. Each CLB output can drive several of the single-length lines, with connections to both the horizontal and vertical Longlines.

The double-length lines (Figure 8) consist of a grid of metal segments twice as long as the single-length lines; i.e, a double-length line runs past two CLBs before entering a Switch Matrix. Double-length lines are grouped in pairs with the Switch Matrices staggered so that each line goes through a Switch Matrix at every other CLB location in that row or column. As with single-length lines, all the CLB inputs except K can be driven from any adjacent double-length line, and each CLB output can drive nearby double-length lines in both the vertical and horizontal planes. Double-length lines provide the most efficient implementation of intermediate length, point-to-point interconnections.

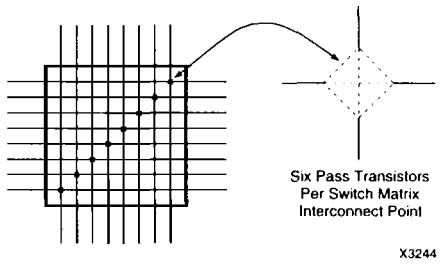


Figure 7. Switch Matrix

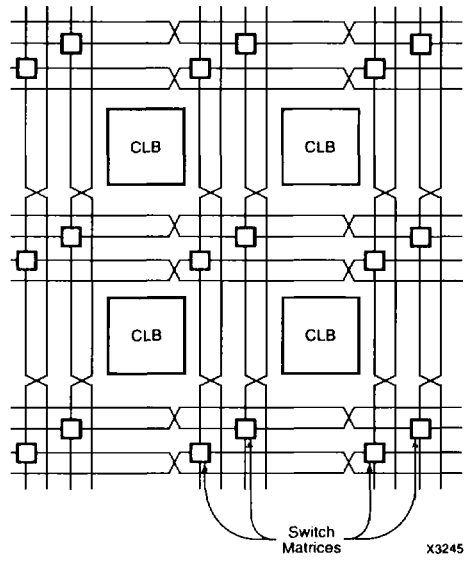


Figure 8. Double-Length Lines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array (Figure 9). Additional vertical longlines can be driven by special global buffers, designed to distribute clocks and other high fanout control signals throughout the array with minimal skew. Longlines are intended for high fan-out, time-critical signal nets. Each Longline has a programmable splitter switch at its center, that can separate the line into two independent routing channels, each running half the width or height of the array. CLB inputs can be driven from a subset of the adjacent Longlines; CLB outputs are routed to the Longlines via 3-state buffers or the single-length interconnected lines.

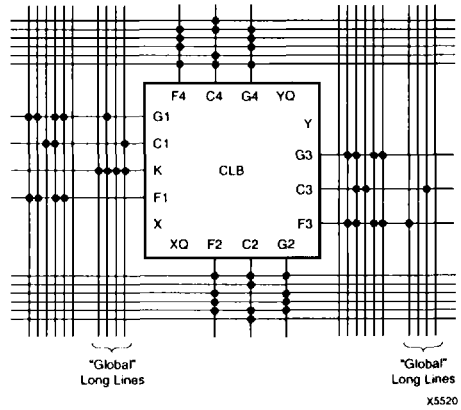


Figure 9. Longline Routing Resources with Typical CLB Connections

Communication between Longlines and single-length lines is controlled by programmable interconnect points at the line intersections. Double-length lines do not connect to other lines.

Three-State Buffers

A pair of 3-state buffers, associated with each CLB in the array, can be used to drive signals onto the nearest horizontal Longlines above and below the block. This feature is also available in the XC3000 generation of LCA devices. The 3-state buffer input can be driven from any X, Y, XQ, or YQ output of the neighboring CLB, or from nearby single-length lines; the buffer enable can come from nearby vertical single-length or Longlines. Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array. These buffers can be used to implement multiplexed or bidirectional buses on the horizontal Longlines. Programmable pull-up resistors attached to both ends of these Longlines help to implement a wide wired-AND function.

Special Longlines running along the perimeter of the array can be used to wire-AND signals coming from nearby IOBs or from internal Longlines.

Taking Advantage of Reconfiguration

LCA devices can be reconfigured to change logic function while resident in the system. This gives the system designer a new degree of freedom, not available with any other type of logic. Hardware can be changed as easily as software. Design updates or modifications are easy. An LCA device can even be reconfigured dynamically to perform different functions at different times. Reconfigurable logic can be used to implement system self diagnostics, create systems capable of being reconfigured for different environments or operations, or implement dual-purpose hardware for a given application. As an added benefit, use of reconfigurable LCA devices simplifies hardware design and debugging and shortens product time-to-market.

Development System

The powerful features of the XC4000 device families require an equally powerful, yet easy-to-use set of development tools. Xilinx provides an enhanced version of the Xilinx Automatic CAE Tools (XACT) optimized for the XC4000 families.

As with other logic technologies, the basic methodology for XC4000 FPGA design consists of three inter-related steps: entry, implementation, and verification. Popular 'generic' tools are used for entry and simulation (for example, Viewlogic System's ViewDraw schematic editor and ViewSim simulator), but architecture-specific tools are needed for implementation.

All Xilinx development system software is integrated under the Xilinx Design Manager (XDM), providing designers with a common user interface regardless of their choice of entry and verification tools. XDM simplifies the selection of command-line options with pull-down menus and on-line help text. Application programs ranging from schematic capture to Partitioning, Placement, and Routing (PPR) can be accessed from XDM, while the program-command sequence is generated and stored for documentation prior to execution. The XMAKE command, a design compilation utility, automates the entire implementation process, automatically retrieving the design's input files and performing all the steps needed to create configuration and report files.

Several advanced features of the XACT system facilitate XC4000 FPGA design. The MEMGEN utility, a memory compiler, implements on-chip RAM within an XC4000 FPGA. Relationally Placed Macros (RPMs) – schematic-based macros with relative locations constraints to guide their placement within the FPGA – help ensure an optimized implementation for common logic functions. XACT-Performance, a feature of the Partition, Place, and Route (PPR) implementation program, allows designers to enter their exact performance requirements during design entry, at the schematic level.

Design Entry

Designs can be entered graphically, using schematic-capture software, or in any of several text-based formats (such as Boolean equations, state-machine descriptions, and high-level design languages).

Xilinx and third-party CAE vendors have developed library and interface products compatible with a wide variety of design-entry and simulation environments. A standard interface-file specification, XNF (Xilinx Netlist File), is provided to simplify file transfers into and out of the XACT development system.

Xilinx offers XACT development system interfaces to the following design environments.

- Viewlogic Systems (ViewDraw, ViewSim)
- Mentor Graphics V7 and V8 (NETED, Quicksim, Design Architect, Quicksim II)
- OrCAD (SDT , VST)
- Synopsys (Design Compiler, FPGA Compiler)
- Xilinx-ABEL
- X-BLOX

Many other environments are supported by third-party vendors. Currently, more than 100 packages are supported.

The schematic library for the XC4000 FPGA reflects the wide variety of logic functions that can be implemented in these versatile devices. The library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and including arithmetic functions,

comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, RAM and ROM memory blocks, multiplexers, shift registers, and barrel shifters.

Designing with macros is as easy as designing with standard SSI/MSI functions. The 'soft macro' library contains detailed descriptions of common logic functions, but does not contain any partitioning or routing information. The performance of these macros depends, therefore, on how the PPR software processes the design. Relationally Placed Macros (RPMs), on the other hand, do contain predetermined partitioning and relative placement information, resulting in an optimized implementation for these functions. Users can create their own library elements – either soft macros or RPMs – based on the macros and primitives of the standard library.

X-BLOX is a graphics-based high-level description language (HDL) that allows designers to use a schematic editor to enter designs as a set of generic modules. The X-BLOX compiler optimizes the modules for the target device architecture, automatically choosing the appropriate architectural resources for each function.

The XACT design environment supports hierarchical design entry, with top-level drawings defining the major functional blocks, and lower-level descriptions defining the logic in each block. The implementation tools automatically combine the hierarchical elements of a design. Different hierarchical elements can be specified with different design entry tools, allowing the use of the most convenient entry method for each portion of the design.

Design Implementation

The design implementation tools satisfy the requirement for an automated design process. Logic partitioning, block placement and signal routing, encompassing the design implementation process, are performed by the Partition, Place, and Route program (PPR). The partitioner takes the logic from the entered design and maps the logic into the architectural resources of the FPGA (such as the logic blocks, I/O blocks, 3-state buffers, and edge decoders). The placer then determines the best locations for the blocks, depending on their connectivity and the required performance. The router finally connects the placed blocks together. The PPR algorithms result in the fully automatic implementation of most designs. However, for demanding applications, the user may exercise various degrees of control over the automated implementation process. Optionally, user-designated partitioning, placement, and routing information can be specified as part of the design entry process. The implementation of highly-structured designs can greatly benefit from the basic floorplanning techniques familiar to designers of large gate arrays.

The PPR program includes XACT-Performance, a feature that allows designers to specify the timing requirements along entire paths during design entry. Timing path analysis routines in PPR then recognize and accommodate the user-specified requirements. Timing requirements can be entered on the schematic in a form directly relating to the system requirements (such as the targeted minimum clock frequency, or the maximum allowable delay on the data path between two registers). So, while the timing of each individual net is not predictable (nor does it need to be), the overall performance of the system along entire signal paths is automatically tailored to match user-generated specifications.

The automated implementation tools are complemented by the XACT Design Editor (XDE), an interactive graphics-based editor that displays a model of the actual logic and routing resources of the FPGA. XDE can be used to directly view the results achieved by the automated tools. Modifications can be made using XDE; XDE also performs checks for logic connectivity and possible design-rule violations.

Design Verification

The high development cost associated with common mask-programmed gate arrays necessitates extensive simulation to verify a design. Due to the custom nature of masked gate arrays, mistakes or last-minute design changes cannot be tolerated. A gate-array designer must simulate and test all logic and timing using simulation software. Simulation describes what happens in a system under worst-case situations. However, simulation is tedious and slow, and simulation vectors must be generated. A few seconds of system time can take weeks to simulate.

Programmable-gate-array users, however, can use in-circuit debugging techniques in addition to simulation. Because Xilinx devices are reprogrammable, designs can be verified in the system in real time without the need for extensive simulation vectors.

The XACT development system supports both simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database. This data can then be sent to the simulator to verify timing-critical portions of the design. Back-annotation – the process of mapping the timing information back into the signal names and symbols of the schematic – eases the debugging effort.

For in-circuit debugging, XACT includes a serial download and readback cable (XChecker) that connects the device in the system to the PC or workstation through an RS232 serial port. The engineer can download a design or a design revision into the system for testing. The designer can also single-step the logic, read the contents of the numerous flip-flops on the device and observe internal logic levels. Simple modifications can be downloaded into the system in a matter of minutes.

The XACT system also includes XDelay, a static timing analyzer. XDelay examines a design's logic and timing to calculate the performance along signal paths, identify possible race conditions, and detect set-up and hold-time violations. Timing analyzers do not require that the user generate input stimulus patterns or test vectors.

Summary

The result of eight years of FPGA design experience and feedback from thousands of customers, the XC4000 families combine architectural versatility, on-chip RAM, increased speed and gate complexity with abundant routing resources and new, sophisticated software to achieve fully automated implementation of complex, high-performance designs.

7400 Equivalents

	# of CLBs
'138	5
'139	2
'147	5
'148	6
'150	5
'151	3
'152	3
'153	2
'154	16
'157	2
'158	2
'160	5
'161	6
'162	8
'163	8
'164	4
'165s	9
'166	5
'168	7
'174	3
'194	5
'195	3
'280	3
'283	8
'298	2
'352	2
'390	3
'518	3
'521	3

Barrel Shifters

brlshft4	4
brlshft8	13

4-Bit Counters

cd4ce	3
cd4cle	5
cd4rle	6
cb4ce	3
cb4cle	6
cb4re	5

8- and 16-Bit Counters

cb8ce	6
cb8re	10
cc16ce	10
cc16cle	11
cc16cled	21

Identity Comparators

comp4	1
comp8	2
comp16	5

Magnitude Comparators

compm4	4
compm8	9
compm16	20

Decoders

d2-4e	2
d3-8e	4
d4-16e	16

Multiplexers

m2-1e	1
m4-1e	1
m8-1e	3
m16-1e	5

Registers

rd4r	2
rd8r	4
rd16r	8

Shift Registers

sr8ce	4
sr16re	8

RAMs

ram 16x4	2

Explanation of counter nomenclature

cb = binary counter
cd = BCD counter
cc = cascadable binary counter
d = bidirectional
l = loadable
x = cascadable
e = clock enable
r = synchronous reset
c = asynchronous clear

Figure 10. CLB Count of Selected XC4000 Soft Macros

Detailed Functional Description

XC4000 and XC4000A Input/Output Blocks

(For XC4000H family, see page 2-82)

The IOB forms the interface between the internal logic and the I/O pads of the LCA device. Under configuration control, the output buffer receives either the logic signal (.out) routed from the internal logic to the IOB, or the complement of this signal, or this same data after it has been clocked into the output flip-flop.

As a configuration option, each flip-flop (CLB or IOB) is initialized as either set or reset, and is also forced into this programmable initialization state whenever the global Set/Reset net is activated after configuration has been completed. The clock polarity of each IOB flip-flop can be configured individually, as can the polarity of the 3-state control for the output buffer.

Each output buffer can be configured to be either fast or slew-rate limited, which reduces noise generation and ground bounce. Each I/O pin can be configured with either an internal pull-up or pull down resistor, or with no internal resistor. Independent of this choice, each IOB has a pull-up resistor during the configuration process.

The 3-state output driver uses a totem pole n-channel output structure. V_{OH} is one n-channel threshold lower than V_{CC}, which makes rise and fall delays more symmetrical.

Family	Per IOB Source	Per IOB Sink	Per IOB Pair Sink	# Slew Modes
XC4000	4	12	24	2
XC4000A	4	24	48	4
XC4000H	4	24*	48	2

*XC4000H devices can sink only 4 mA configured for SoftEdge mode

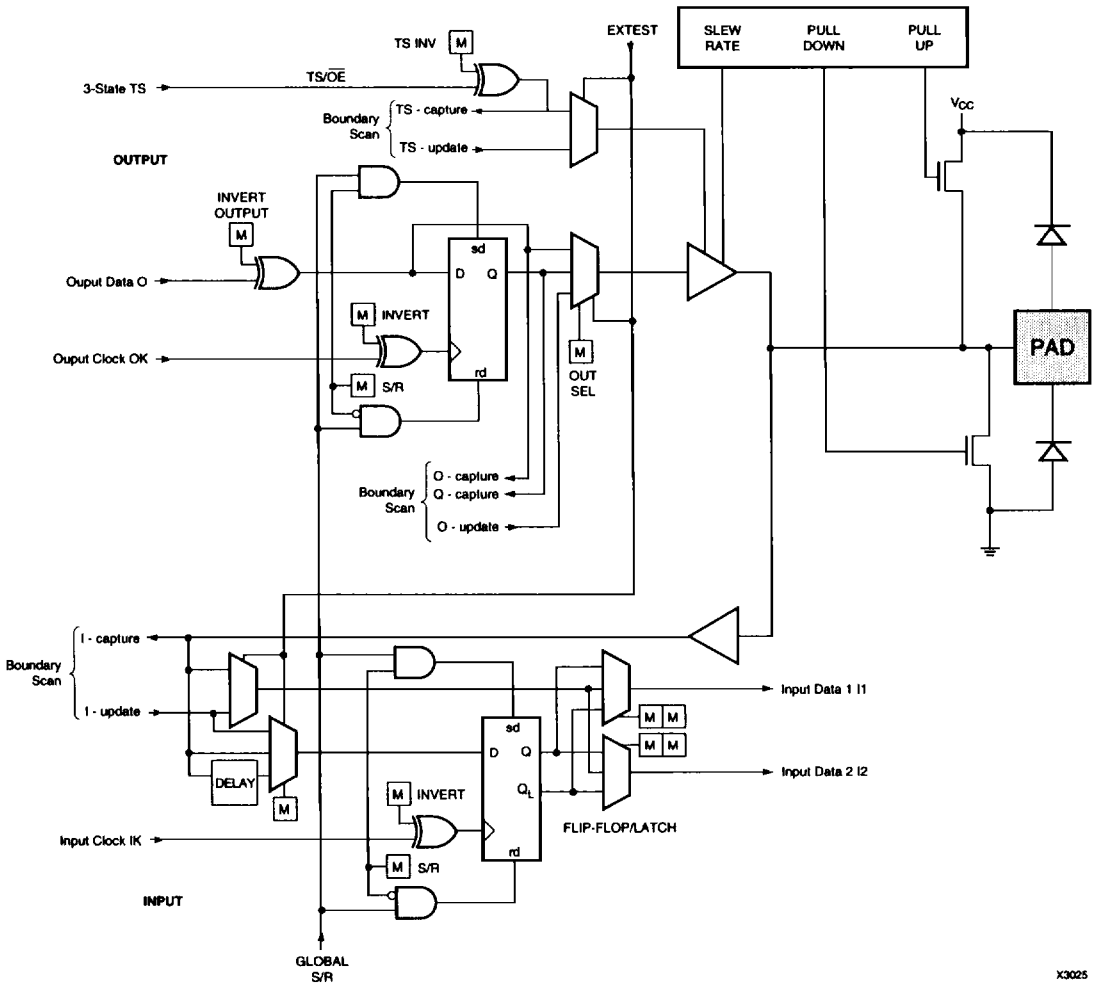


Figure 11. XC4000 and XC4000A I/O Block

The inputs drive TTL-compatible buffers with 1.2-V input threshold and a slight hysteresis of about 300 mV. These buffers drive the internal logic as well as the D-input of the input flip-flop.

Under configuration control, the set-up time of this flip-flop can be increased so that normal clock routing does not result in a hold-time problem. Note that the input flip-flop set-up time is defined between the data measured at the device I/O pin and the clock input at the IOB. Any clock routing delay must, therefore, be subtracted from this set-up time to arrive at the real set-up time requirement on the device pins. A short specified set-up time might, therefore, result in a negative set-up time at the device pins, i.e. a hold-time requirement, which is usually undesirable. The default long set-up time can tolerate more clock delay without causing a hold-time requirement. For faster input register setup time, with non-zero hold, attach a "NODELAY" property to the flip-flop. The exact method to accomplish this depends on the design entry tool.

The input block has two connections to the internal logic, I1 and I2. Each of these is driven either by the incoming data, by the master or by the slave of the input flip-flop.

Wide Decoders

The periphery of the chip has four wide decoder circuits at each edge (two in the XC4000A). The inputs to each decoder are any of the I1 signals on that edge plus one local interconnect per CLB row or column. Each decoder generates High output (resistor pull-up) when the AND condition of the selected inputs, or their complements, is true. This is analogous to the AND term in typical PAL devices. Each decoder can be split at its center.

The decoder outputs can drive CLB inputs so they can be combined with other logic, or to form a PAL-like AND/OR structure. The decoder outputs can also be routed directly to the chip outputs. For fastest speed, the output should be on the same chip edge as the decoder.

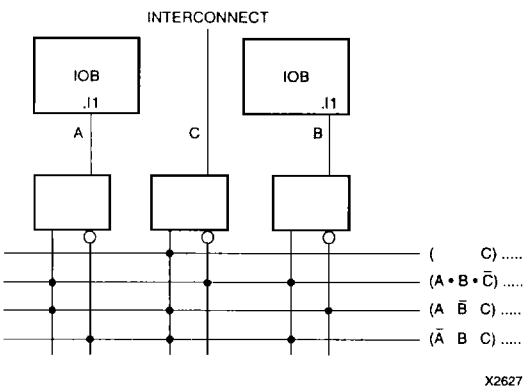


Figure 12. Example of Edge Decoding. Each row or column of CLBs provide up to three variables (or their complements)

Configurable Logic Blocks

Configurable Logic Blocks implement most of the logic in an LCA device. Two 4-input function generators (F and G) offer unrestricted versatility. A third function generator (H) can combine the outputs of F and G with a ninth input variable, thus implementing certain functions of up to nine variables, like parity check or expandable-identity comparison of two sets of four inputs.

The four control inputs C1 through C4 can each generate any one of four logic signals, used in the CLB.

- Enable Clock, Asynchronous Preset/Reset, DIN, and H1, when the memory function is disabled, or
- Enable Clock, Write Enable, D0, and D1, when the memory function is enabled.

Since the function-generator outputs are brought out independently of the flip-flop outputs, and DIN and H1 can be used as direct inputs to the two flip-flops, the two combinatorial and the two sequential functions in the CLB can be used independently. This versatility increases logic density and simplifies routing.

The asynchronous flip-flop input can be configured as either set or reset. This configuration option also determines the state in which the flip-flops become operational after configuration, as well as the effect of an externally or internally applied Set/Reset during normal operation.

Fast Carry Logic

The CLBs can generate the arithmetic-carry output for incoming operands, and can pass this extra output on to the next CLB function generator above or below. This connection is independent of normal routing resources and it is, presently, only supported by Hard Macros. A later software release will accommodate Soft Macros and will permit graphic editing of the fast logic circuitry. This fast carry logic is one of the most significant improvements in the XC4000 families, speeding up arithmetic and counting into the 60-MHz range.

Using Function Generators as RAMs

Using XC4000 devices, the designer can write into the latches that hold the configuration content of the function generators. Each function generator can thus be used as a small Read/Write memory, or RAM. The function generators in any CLB can be configured in three ways.

- Two 16 x 1 RAMs with two data inputs and two data outputs – identical or, if preferred, different addressing for each RAM
- One 32 x 1 RAM with one data input and one data output
- One 16 x 1 RAM plus one 5-input function generator

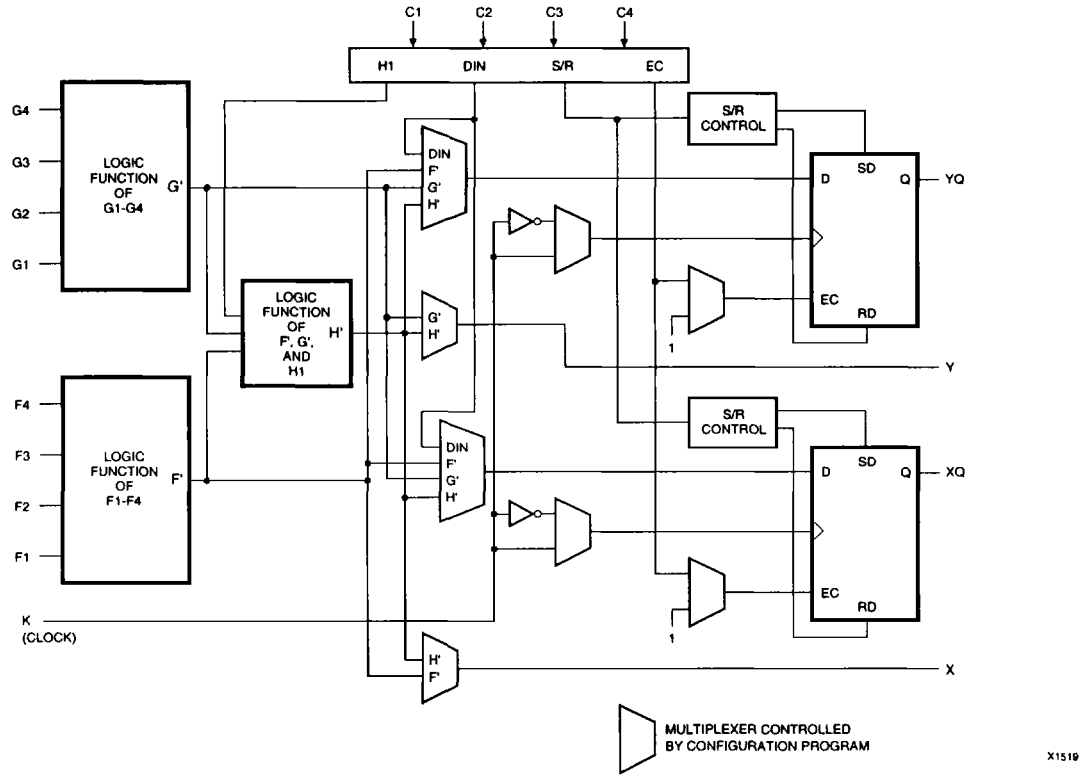


Figure 13. Simplified Block Diagram of XC4000 Configurable Logic Block

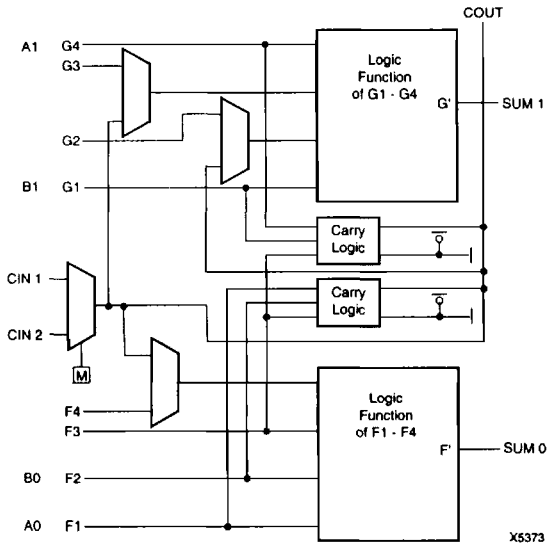


Figure 14. Fast Carry Logic in Each CLB

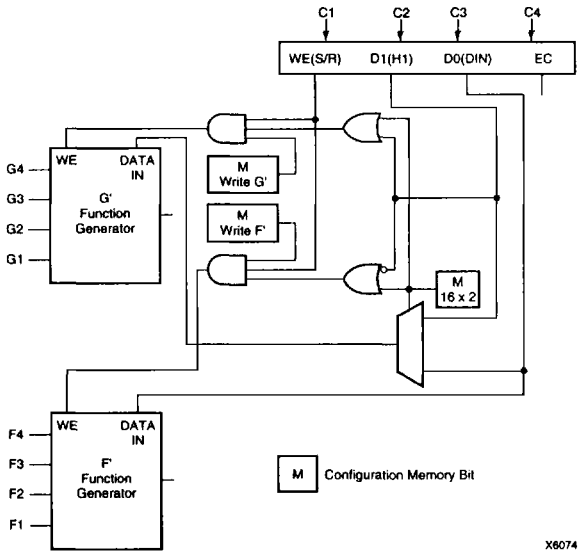


Figure 15. CLB Function Generators Can Be Used as Read/Write Memory Cells

Boundary Scan

Boundary Scan is becoming an attractive feature that helps sophisticated systems manufacturers test their PC boards more safely and more efficiently. The XC4000 family implements IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST Boundary-Scan instructions. When the Boundary-Scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions.

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their electronic design. This structure is easily implemented with the serial and/or parallel connections of a four-pin interface on any Boundary-Scan-compatible IC. By exercising these signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This is an improvement over bed-of-nails testing. It avoids the need to overdrive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Xilinx part.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. A register operation begins with a *capture* where a set of data is parallel loaded into the designated register for shifting out. The next state is *shift*, where captured data are shifted out while the desired data are shifted in. A number of states are provided for Wait operations. The last state of a register sequence is the *update* where the shifted content of the register is loaded into the appropriate instruction- or data-holding register, either for instruction-register decode or for data-register pin control.

The primary data register is the Boundary-Scan register. For each IOB pin in the LCA device, it includes three bits of shift register and three *update* latches for: in, out and 3-state control. Non-IOB pins have appropriate partial bit population for in or out only. Each Extest Capture captures all available input pins.

The other standard data register is the single flip-flop *bypass* register. It resynchronizes data being passed through a device that need not be involved in the current scan operation. The LCA device provides two user nets (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding nets (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and Run-test-idle is also provided (BSCAN.IDLE).

The XC4000 Boundary Scan instruction set also includes instructions to configure the device and read back the configuration data.

Table 4. Boundary Scan Instruction

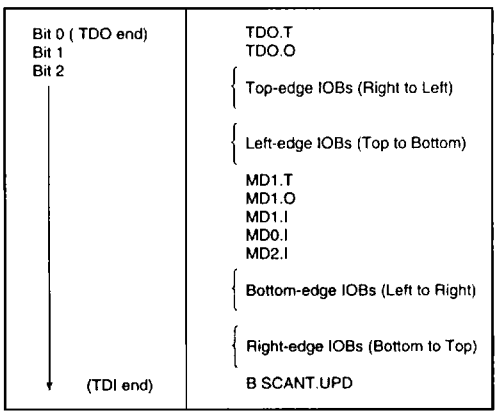
Instruction I_2	I_1	I_0	Test Selected	TDO Source	I/O Data Source
0	0	0	Extest	DR	DR
0	0	1	Sample/Preload	DR	Pin/Logic
0	1	0	User 1	TDO1	Pin/Logic
0	1	1	User 2	TDO2	Pin/Logic
1	0	0	Readback	Readback Data	Pin/Logic
1	0	1	Configure	DOUT	Disabled
1	1	0	Reserved	—	—
1	1	1	Bypass	Bypass Reg	Pin/Logic

X2679

Bit Sequence

The bit sequence within each IOB is: in, out, 3-state. From a cavity-up (XDE) view of the chip, starting in the upper right chip corner, the Boundary-Scan data-register bits have the following order.

Table 5. Boundary Scan Order



X6075

The data register also includes the following non-pin bits: TDO.T, and TDO.I, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD which is always the last bit of the data register. These three Boundary-Scan bits are special-purpose Xilinx test signals. PROGRAM, CCLK and DONE are not included in the Boundary-Scan register. For more information regarding Boundary Scan, refer to XAPP 017.001, *Boundary Scan in XC4000 Devices*.

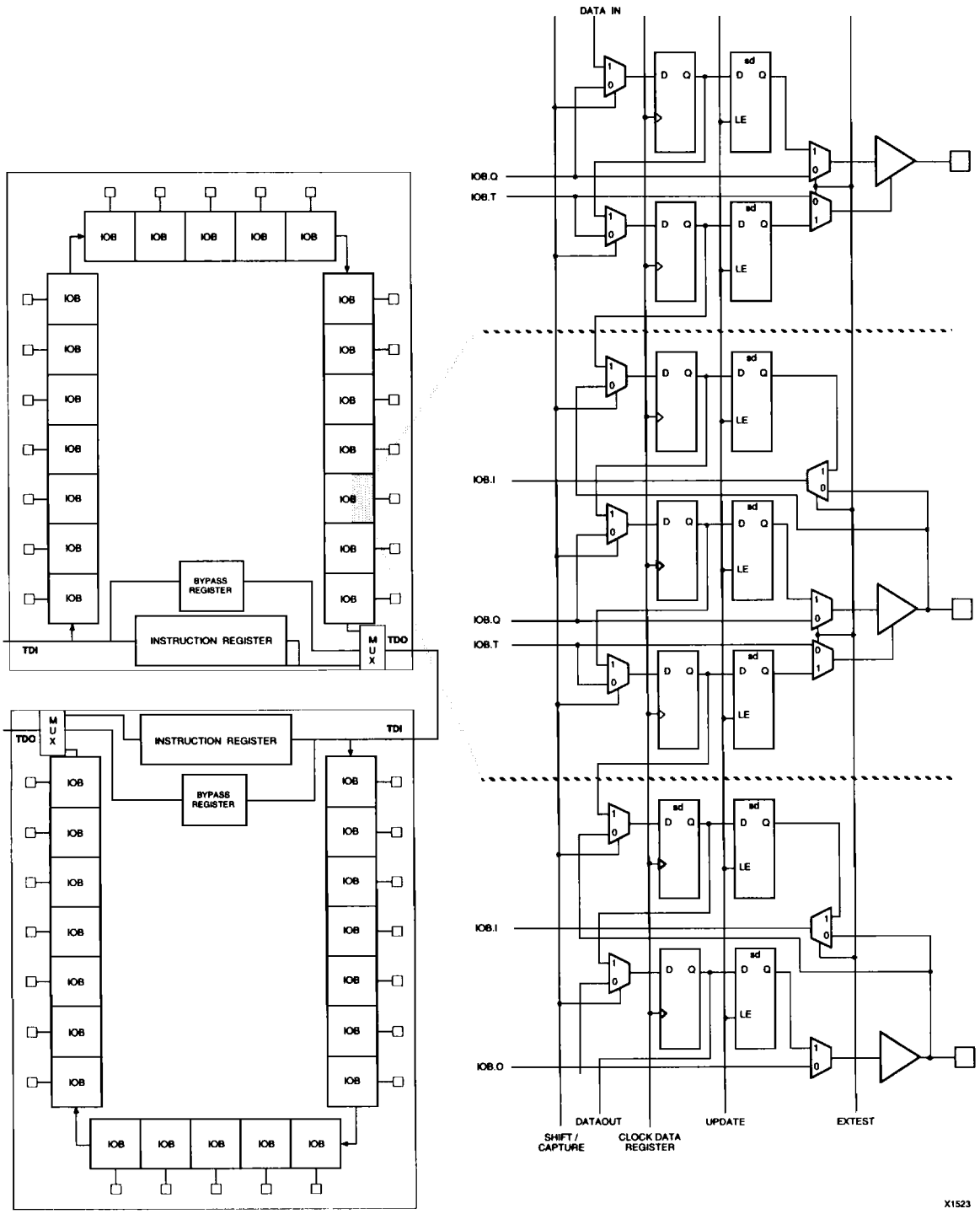


Figure 16. XC4000 Boundary Scan Logic. Includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Interconnects

The XC4000 families use a hierarchy of interconnect resources.

- General purpose single-length and double-length lines offer fast routing between adjacent blocks, and highest flexibility for complex routes, but they incur a delay every time they pass through a switch matrix.
- Longlines run the width or height of the chip with negligible delay variations. They are used for signal distribution over long distances. Some Horizontal Longlines can be driven by 3-state or open-drain drivers, and can thus implement bidirectional buses or wired-AND decoding.
- Global Nets are optimized for the distribution of clock and time-critical or high-fan-out control signal. Four pad-driven Primary Global Nets offer shortest delay and negligible skew. Four pad-driven Secondary Global Nets have slightly longer delay and more skew due to heavier loading.

Each CLB column has four dedicated Vertical Longlines, each of these lines has access to a particular Primary Global Net, or to any one of the Secondary Global Nets. The Global Nets avoid clock skew and potential hold-time problems. The user must specify these Global Nets for all timing-sensitive global signal distribution.

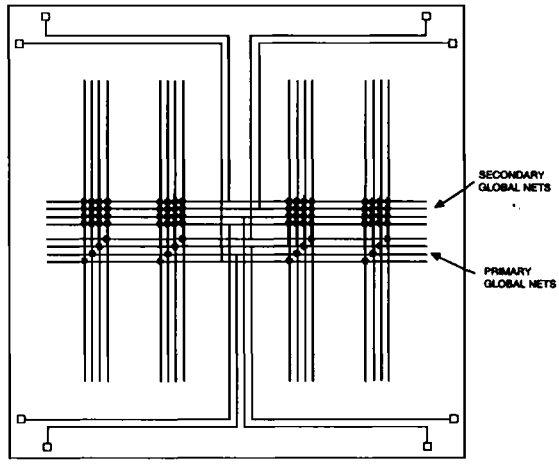
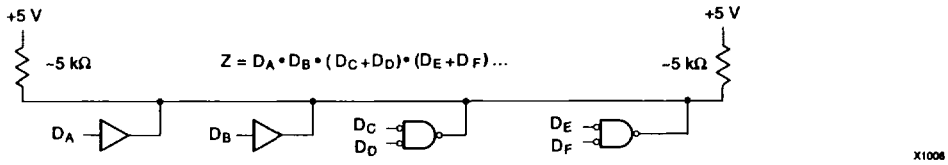
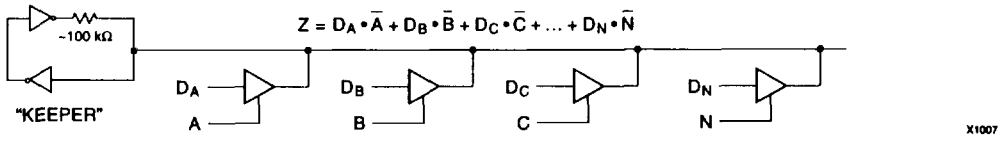


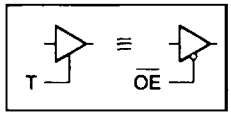
Figure 17. XC4000 Global Net Distribution. Four Lines per Column; Eight Inputs in the Four Chip Corners.



Open Drain Buffers Implement a Wired-AND Function. When all the buffer inputs are High the pull-up resistor(s) provide the High output.



3-State Buffers Implement a Multiplexer. The selection is accomplished by the buffer 3-state signal.



Active High T is Identical to Active Low Output Enable.

Figure 18. TBUFs Driving Horizontal Longlines.

Oscillator

An internal oscillator is used for clocking of the power-on time-out, configuration memory clearing, and as the source of CCLK in Master modes. This oscillator signal runs at a nominal 8 MHz and varies with process, V_{CC} and temperature between 10 MHz max and 4 MHz min. This signal is available on an output control net (OSCO) in the upper right corner of the chip, if the oscillator-run control bit is enabled in the configuration memory. Two of four resynchronized taps of the power-on time-out divider are also available on OSC1 and OSC2. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the ripple divider. This can provide output signals of approximately 500 kHz,16 kHz, 490 Hz and 15 Hz.

Special Purpose Pins

The mode pins are sampled prior to configuration to determine the configuration mode and timing options. After configuration, these pins can be used as auxiliary connections: Mode 0 (MD0.I) and Mode 2 (MD2.I) as inputs and Mode 1 (MD1.O and MD1.T) as an output. The XACT development system will not use these resources unless they are explicitly specified in the design entry. These dedicated nets are located in the lower left chip corner and are near the readback nets. This allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

Table 6. Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel up	1	0	0	output	Byte-Wide, 00000 ↑
Master Parallel down	1	1	0	output	Byte-Wide, 3FFFF↓
Peripheral Synchr.	0	1	1	input	Byte-Wide
Peripheral Asynchr.	1	0	1	output	Byte-Wide
Reserved	0	1	0	—	—
Reserved	0	0	1	—	—

Peripheral Synchronous can be considered Slave Parallel

Configuration

Configuration is the process of loading design-specific programming data into one or more LCA devices to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. The XC4000 families use about 350 bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The XACT development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Modes

The XC4000 families have six configuration modes selected by a 3- bit input code applied to the M0, M1, and M2 inputs. There are three self-loading Master modes, two Peripheral modes and the Serial Slave mode used primarily for daisy-chained devices. During configuration, some of the I/O pins are used temporarily for the configuration process. See Table 6.

For a detailed description of these configuration modes, see pages 2-32 through 2-41.

Master

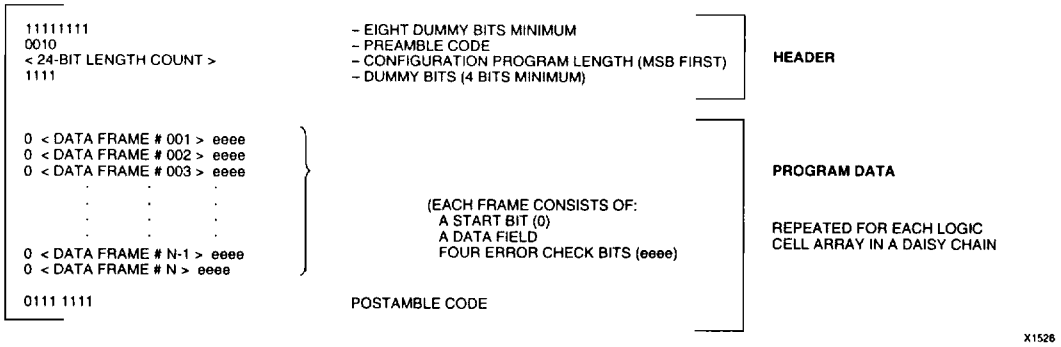
The Master modes use an internal oscillator to generate CCLK for driving potential slave devices, and to generate address and timing for external PROM(s) containing the configuration data. Master Parallel (up or down) modes generate the CCLK signal and PROM addresses and receive byte parallel data, which is internally serialized into the LCA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, to be compatible with different microprocessor addressing conventions. The Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

Peripheral

The two Peripheral modes accept byte-wide data from a bus. A READY/BUSY status is available as a handshake signal. In the asynchronous mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

Serial Slave

In the Serial Slave mode, the LCA device receives serial-configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK. Multiple slave devices with identical configurations can be wired with parallel DIN inputs so that the devices can be configured simultaneously.



Device	XC4002A	XC4003A	XC4003/H	XC4004A	XC4005A	XC4005/H	XC4006	XC4008	XC4010/D	XC4013/D	XC4020	XC4025
Gates	2,000	3,000	3,000	4,000	5000	5,000	6,000	8,000	10,000	13,000	20,000	25,000
CLBs	64	100	100	144	196	196	256	324	400	576	784	1,024
(Row x Col)	(8 x 8)	(10 x 10)	(10 x 10)	(12 x 12)	(14 x 14)	(14 x 14)	(16 x 16)	(18 x 18)	(20 x 20)	(24 x 24)	(28 x 28)	(32 x 32)
IOBs	64	80	80/.160	96	112	112 (192)	128	144	160	192	224	256
Flip-flops	256	360	360/300	480	616	616 (392)	768	936	1,120	1,536	2,016	2,560
Horizontal TBUF Longlines	16	20	20	24	28	28	32	36	40	48	56	64
TBUFs/Longline	10	12	12	14	16	16	18	20	22	26	30	34
Bits per Frame	102	122	126	142	162	166	186	206	226	266	306	346
Frames	310	374	428	438	502	572	644	716	788	932	1,076	1,220
Program Data	31,628	45,636	53,936	62,204	81,332	94,960	119,792	147,504	178,096	247,920	329,264	422,128
PROM size (bits)	31,668	45,676	53,976	62,244	81,372	95,000	119,832	147,544	178,136	247,960	329,304	422,168

XC4000, 4000H: Bits per Frame = (10 x number of Rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits
Number of Frames = (36 x number of Columns) + 26 for the left edge + 41 for the right edge + 1
XC4000A: Bits per Frame = (10 x number of Rows) + 6 for the top + 10 for the bottom + 1 + 1 start bit + 4 error check bits
Number of Frames = (32 x number of Columns) + 21 for the left edge + 32 for the right edge + 1
Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
PROM Size = Program Data + 40
The user can add more "one" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits, but the Length Count value **must** be adjusted for all such extra "one" bits, even for leading extra ones at the beginning of the header.

Figure 19. Internal Configuration Data Structure.

Format

The configuration-data stream begins with a string of ones, a 0010 preamble code, a 24-bit length count, and a four-bit separator field of ones. This is followed by the actual configuration data in frames, each starting with a zero bit and ending with a four-bit error check. For each XC4XXX device, the MakeBits software allows a selection of CRC or non-CRC error checking. The non-CRC error checking tests for a 0110 end of frame field for each frame of a selected LCA device. For CRC error checking, MakeBits software calculates a running CRC of inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an LCA device includes the last seven data bits. Detection of an error results in suspension of data loading and the pulling down of the $\overline{\text{INIT}}$ pin. In master modes, CCLK and address signals continue to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin or cycling V_{CC}. The length and number of frames depend on the device type. Multiple LCA devices can be connected in a daisy chain by wiring their CCLK pins in parallel and connecting the DOUT of each to the DIN of the next. The lead-master LCA device and following slaves each passes resynchronized configuration data coming from a single source. The Header data, including the length count, is passed through and is captured by each LCA

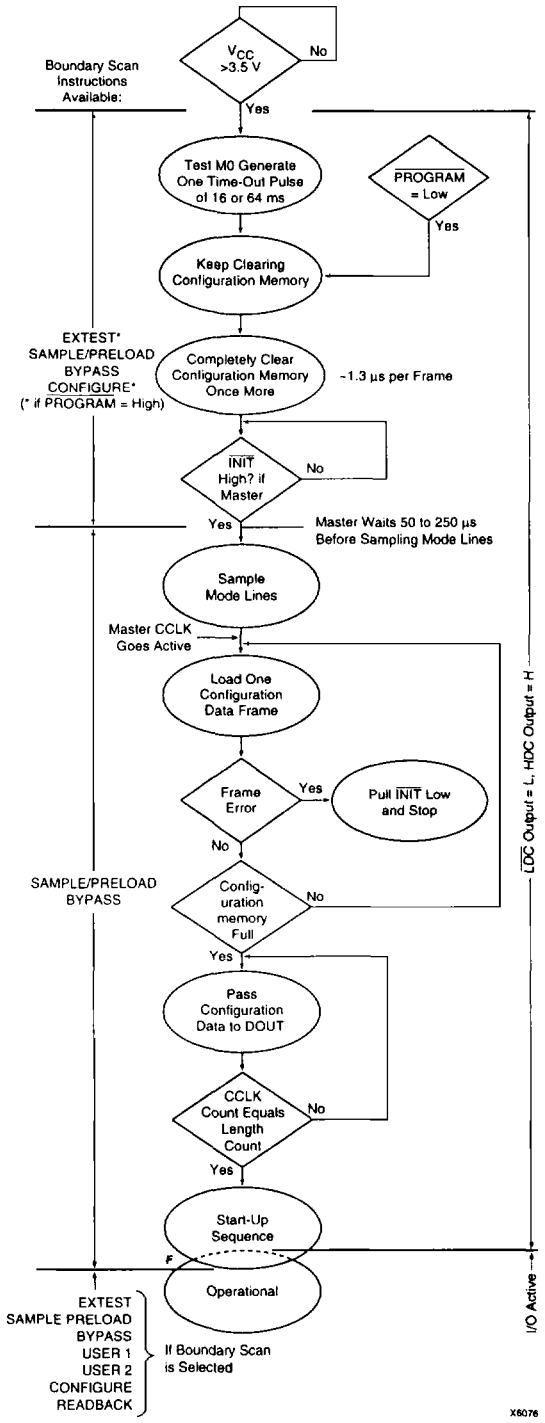


Figure 20. Start-up Sequence

device when it recognizes the 0010 preamble. Following the length-count data, any LCA device outputs a High on DOUT until it has received its required number of data frames.

After an LCA device has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the LCA device(s) begin the start-up sequence and become operational together.

Configuration Sequence

Configuration Memory Clear

When power is first applied or reapplied to an LCA device, an internal circuit forces initialization of the configuration logic. When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a nominal 16-ms time delay is started (four times longer when M0 is Low, i.e., in Master mode). During this time delay, or as long as the $\overline{\text{PROGRAM}}$ input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator. At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the $\overline{\text{PROGRAM}}$ pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the $\overline{\text{INIT}}$ input.

Initialization

During initialization and configuration, user pins HDC, $\overline{\text{LDC}}$ and $\overline{\text{INIT}}$ provide status outputs for system interface. The outputs, $\overline{\text{LDC}}$, $\overline{\text{INIT}}$ and DONE are held Low and HDC is held High starting at the initial application of power. The open drain $\overline{\text{INIT}}$ pin is released after the final initialization pass through the frame addresses. There is a deliberate delay of 50 to 250 µs before a Master-mode device recognizes an inactive $\overline{\text{INIT}}$. Two internal clocks after the $\overline{\text{INIT}}$ pin is recognized as High, the LCA device samples the three mode lines to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count, i.e., the total number of configuration clocks needed to load the total configuration data. After the preamble and the length count have been passed through to all devices in the daisy chain, DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Each frame has a Low start bit followed by the frame-configura-

tion data bits and a 4-bit frame error field. If a frame data error is detected, the LCA device halts loading, and signals the error by pulling the open-drain $\overline{INIT}$ pin Low.

After all configuration frames have been loaded into an LCA device, DOUT again follows the input data so that the remaining data is passed on to the next device.

Start-Up

Start-up is the transition from the configuration process to the intended user operation. This means a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic "wakes up" gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset or Set at the right time.

Figure 21 describes Start-up timing for the three Xilinx families in detail.

The **XC2000** family goes through a fixed sequence:

DONE goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The **XC3000A** family offers some flexibility: DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The **XC4000** family offers additional flexibility: The three events, DONE going High, the internal Reset/Set being de-activated, and the user I/O going active, can all occur in any arbitrary sequence, each of them one CCLK period before or after, or simultaneous with, any of the other.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset/Set is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 21, but the designer can modify it to meet particular requirements.

The XC4000 family offers another start-up clocking option: The three events described above don't have to be triggered by CCLK, they can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

The XC4000 family introduces an additional option: When this option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the Start-up sequence, until DONE is released and has gone High. This option can be used to force synchronization of several LCA devices to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since INIT went High equals the loaded value of the length count. The next rising clock edge sets a flip-flop Q0 (see Figure 22), the leading bit of a 5-bit shift register.

The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output,
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDed with DONE pins of other LCA devices or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called "Start-up Timing Synchronous to Done In" and labeled: CCLK_SYNC or UCLK_SYNC. When DONE is not used as an input, the operation is called Start-up Timing Not Synchronous to DONE In, and is labeled CCLK_NOSYNC or UCLK_NOSYNC. These labels are not intuitively obvious.

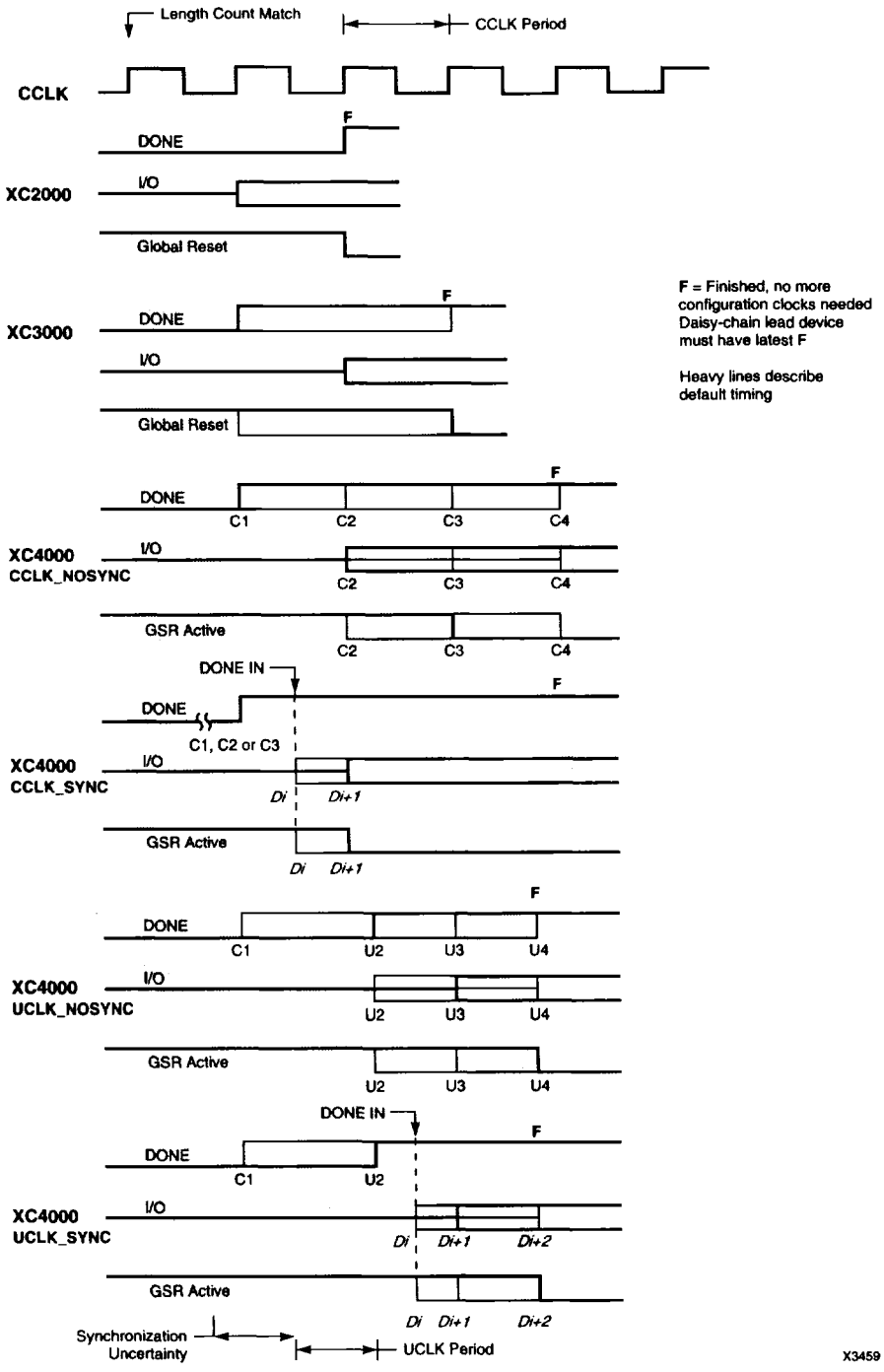
As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK.

Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in Figure 21 show the default timing which is compatible with XC2000 and XC3000 devices using early DONE and late Reset.The thin lines indicate all other possible timing options.

Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.



Note: Thick lines are default option.

Figure 21. Start-up Timing

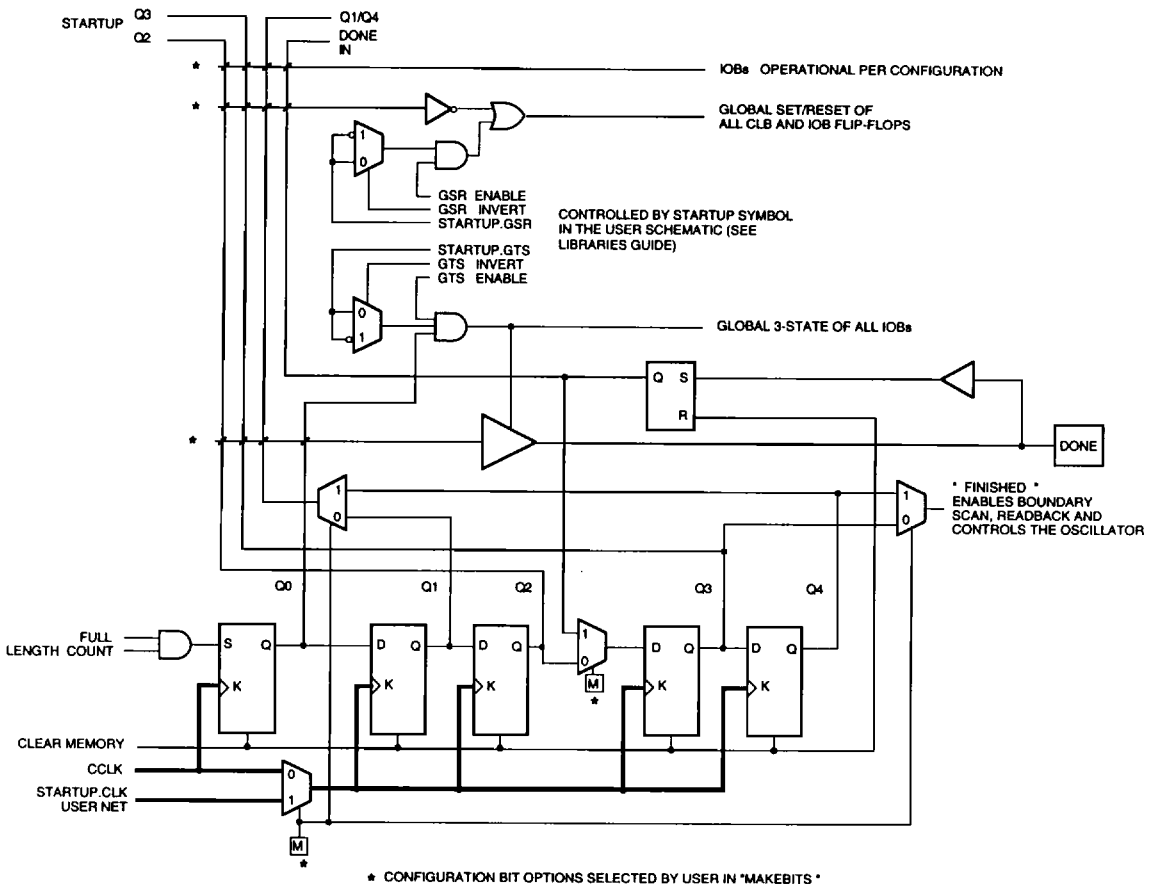


Figure 22. Start-up Logic

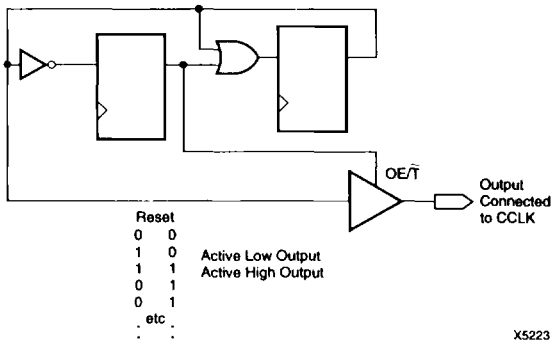
X1528

All Xilinx FPGAs of the XC2000, XC3000, XC4000 families use a compatible bitstream format and can, therefore, be connected in a daisy-chain in an arbitrary sequence. There is however one limitation. The lead device must belong to the highest family in the chain. If the chain contains XC4000 devices, the master cannot be an XC2000 or XC3000 device; if the daisy-chain contains XC3000 devices, the master cannot be an XC2000 device. The reason for this rule is shown in Figure 21 on the previous page. Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of Figure 21. The master device will then drive additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F.

Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal RESET was released. The user has some control over the relative timing of these events and can, therefore, make sure that they occur early enough.

But, for XC4000, not reaching F means that READBACK cannot be initiated and most Boundary Scan instructions cannot be used.This limitation has been criticized by designers who want to use an inexpensive lead device in peripheral mode and have the more precious I/O pins of the XC4000 devices all available for user I/O. Here is a solution for that case.

One CLB and one IOB in the lead XC3000 device are used to generate the additional CCLK pulse required by the XC4000 devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates



the extra CCLK pulse. This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as available clock source. Obviously, this XC3000 master device must be configured with late Internal Reset, which happens to be the default option.

Using Global Set/Reset and Global 3-State Nets
The global Set/Reset (STARTUP.GSR) net can be driven by the user at any time to re-initialize all CLBs and IOBs to the same state they had at the end of configuration. For CLBs that is the same state as the one driven by the individually programmable asynchronous Set/Reset inputs. The global 3-state net (STARTUP.GTS), whenever activated after configuration is completed, forces all LCA outputs to the high-impedance state, unless Boundary Scan is enabled and is executing an EXTEST instruction.

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback reports not only the downloaded configuration bits, but can also include the present state of the device represented by the content of all used flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

XC4000 Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net. Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Note that, in the XC4000 families, data is not inverted with respect to configuration the way it is in XC2000 and XC3000 families.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RIP returns Low.

Readback options are: Read Capture, Read Abort, and Clock Select.

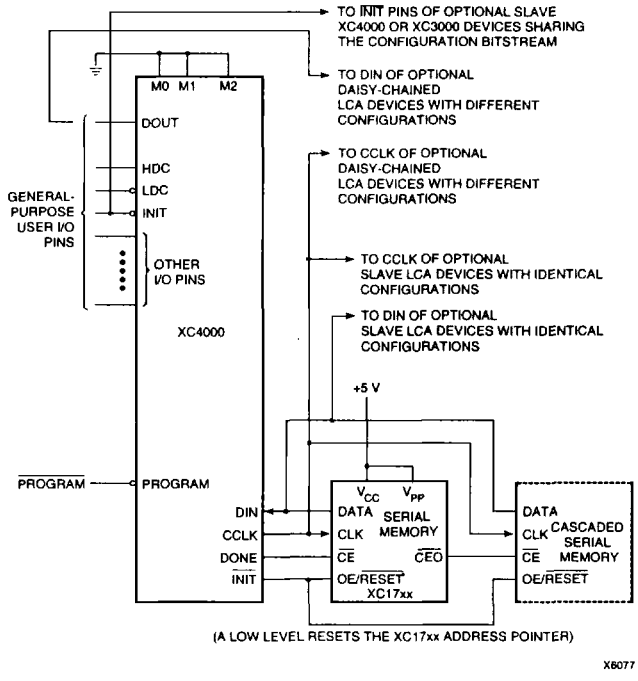
Read Capture
When the Readback Capture option is selected, the readback data stream includes sampled values of CLB and IOB signals imbedded in the data stream. The rising edge of RDBK.TRIG located in the lower-left chip corner, captures, in latches, the inverted values of the four CLB outputs and the IOB output flip-flops and the input signals I1, I2. When the capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in readback, since they directly overwrite the F and G function-table configuration of the CLB.

Read Abort
When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the readback operation and prepares the logic to accept another trigger. After an aborted readback, additional clocks (up-to-one readback clock per configuration frame) may be required to re-initialize the control logic. The status of readback is indicated by the output control net (RDBK.RIP).

Clock Select
Readback control and data are clocked on rising edges of RDBK.CLK located in the lower right chip corner. CCLK is an optional clock. If Readback must be inhibited for security reasons, the readback control nets are simply not connected.

XChecker
The XChecker Universal Download/Readback Cable and Logic Probe uses the Readback feature for bitstream verification and for display of selected internal signals on the PC or workstation screen, effectively as a low-cost in-circuit emulator.

Master Serial Mode



In Master Serial mode, the CCLK output of the lead LCA device drives a Xilinx Serial PROM that feeds the LCA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. This puts the next data bit on the SPROM data output, connected to the LCA DIN pin. The lead LCA device accepts this data on the subsequent rising CCLK edge.

The lead LCA device then presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next LCA device in the daisy-chain accepts data on the subsequent rising CCLK edge. The user can specify Fast ConfigRate, which starting somewhere in the first frame, increases the CCLK frequency eight times, from a value between 0.5 and 1.25 MHz, to a value between 4 and 10 MHz. Note that most Serial PROMs are not compatible with this high frequency.

The SPROM $\overline{CE}$ input can be driven from either $\overline{LDC}$ or DONE. Using $\overline{LDC}$ avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but $\overline{LDC}$ is then restricted to be a permanently High user output. Using DONE can also avoid contention on DIN, provided the early DONE option is invoked.

How to Delay Configuration After Power-Up

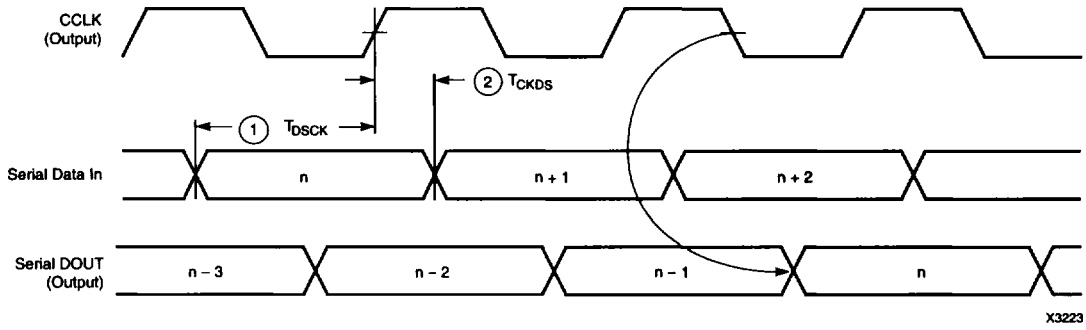
There are two methods to delay configuration after power-up: Put a logic Low on the $\overline{PROGRAM}$ input, or pull the bidirectional $\overline{INIT}$ pin Low, using an open-collector (open-drain) driver. (See also Figure 20 on page 2-27.)

A Low on the $\overline{PROGRAM}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{PROGRAM}$ is Low, the XC4000 device keeps clearing its configuration memory. When $\overline{PROGRAM}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the INIT input is not externally held Low. Note that a Low on the $\overline{PROGRAM}$ input automatically forces a Low on the $\overline{INIT}$ output.

Using an open-collector or open-drain driver to hold $\overline{INIT}$ Low before the beginning of configuration, causes the LCA device to wait after having completed the configuration memory clear operation. When $\overline{INIT}$ is no longer held Low

externally, the device determines its configuration mode by capturing its status inputs, and is ready to start the configuration process. A master device waits an additional up to 250 µs to make sure that all slaves in the potential daisy-chain have seen $\overline{INIT}$ being High.

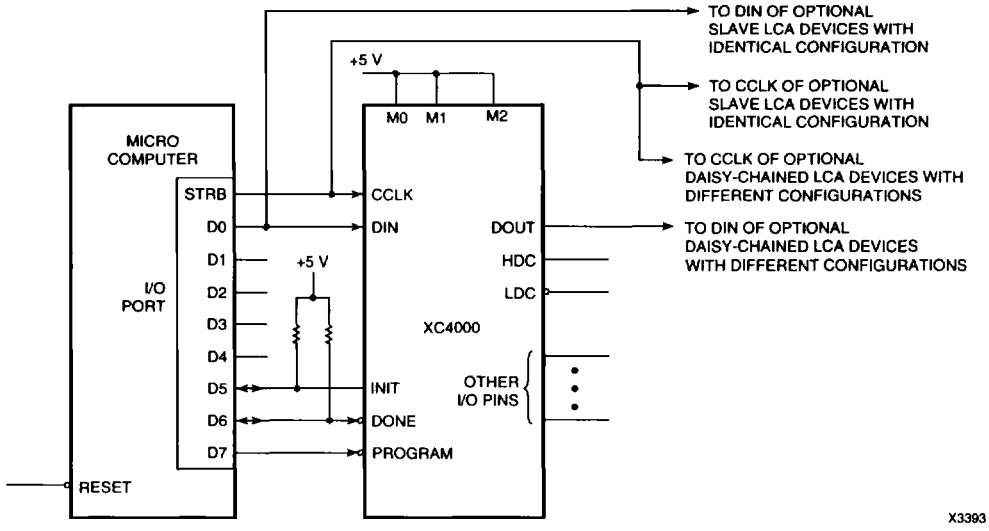
Master Serial Mode Programming Switching Characteristics



	Description	Symbol		Min	Max	Units
CCLK	Data In setup	1	T_{DSCK}	20		ns
	Data In hold	2	T_{CKDS}	0		ns

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling $\overline{PROGRAM}$ Low until V_{CC} is valid.
2. Configuration can be controlled by holding $\overline{INIT}$ Low with or until after the $\overline{INIT}$ of all daisy-chain slave mode devices is High.
3. Master-serial-mode timing is based on testing in slave mode.

Slave Serial Mode



In Slave Serial mode, an external signal drives the CCLK input(s) of the LCA device(s). The serial configuration bitstream must be available at the DIN input of the lead LCA device a short set-up time before each rising CCLK edge. The lead LCA device then presents the preamble data (and all data that overflows the lead device) on its DOUT pin.

There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next LCA device in the daisy-chain accepts data on the subsequent rising CCLK edge.

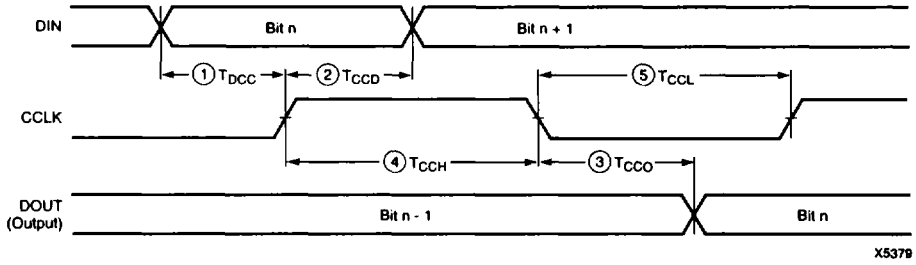
How to Delay Configuration After Power-Up

There are two methods to delay configuration after power-up: Put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See also Figure 20 on page 2-27.)

A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the XC4000 device keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the INIT input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output.

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of configuration, causes the LCA device to wait after having completed the configuration memory clear operation. When $\overline{\text{INIT}}$ is no longer held Low externally, the device determines its configuration mode by capturing its status inputs, and is ready to start the configuration process. A master device waits an additional max 250 µs to make sure that all slaves in the potential daisy-chain have seen $\overline{\text{INIT}}$ being High.

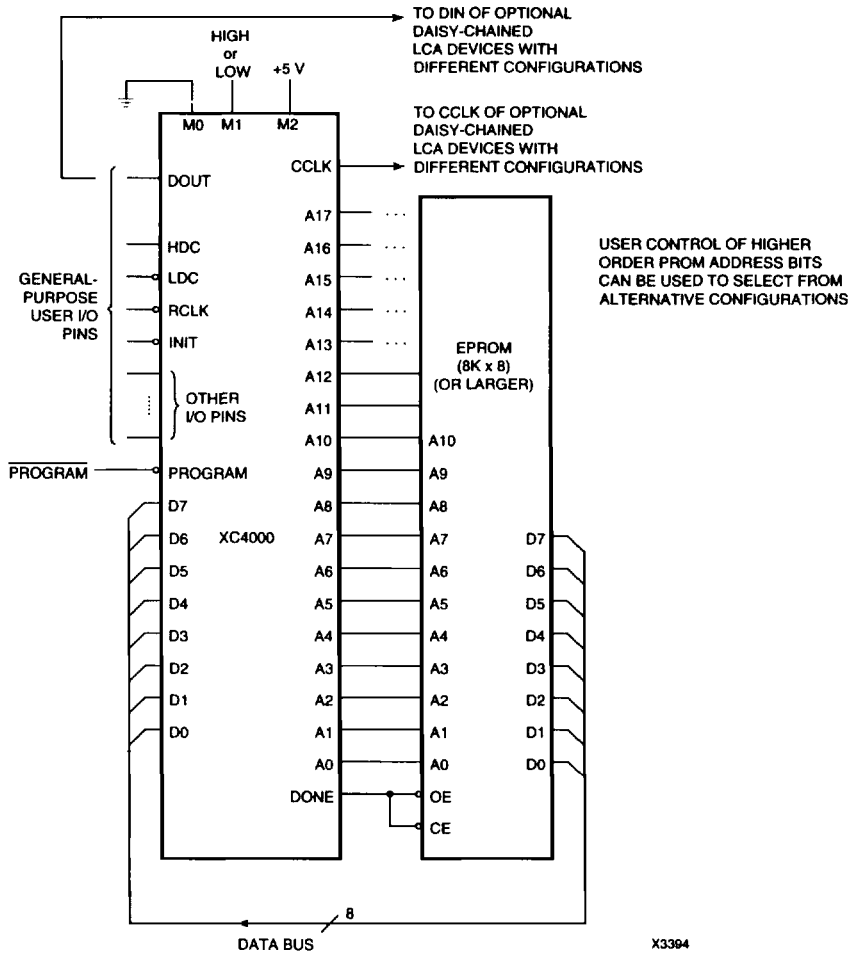
Slave Serial Mode Programming Switching Characteristics



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the INIT of all daisy-chained LCA devices is High.

Master Parallel Mode



In Master Parallel mode, the lead LCA device directly addresses an industry-standard byte-wide EPROM, and accepts eight data bits right before incrementing (or decrementing) the address outputs.

The eight data bits are serialized in the lead LCA device, which then presents the preamble data (and all data that overflows the lead device) on the DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data (and also changes the EPROM address) until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next LCA device in the daisy-chain accepts data on the subsequent rising CCLK edge.

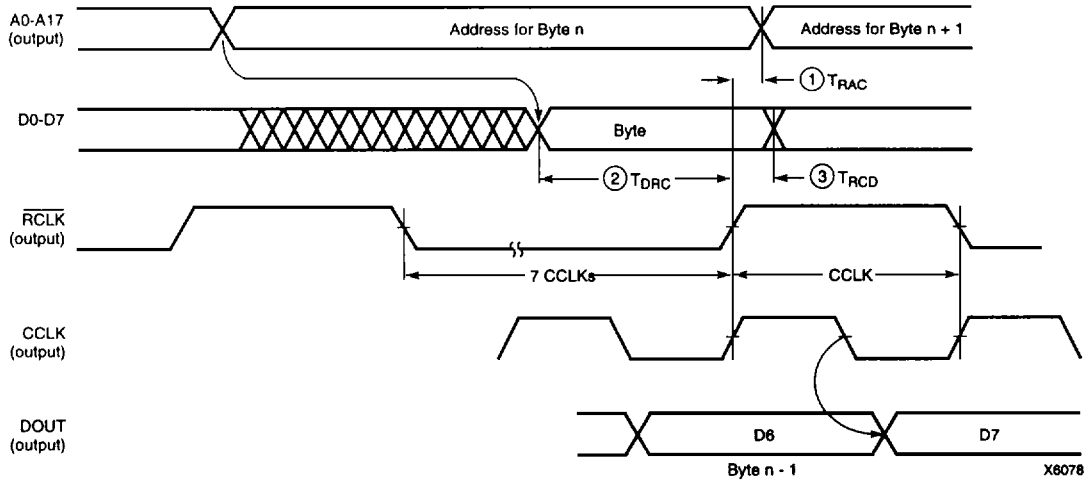
How to Delay Configuration After Power-Up

There are two methods to delay configuration after power-up: Put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See also Figure 20 on page 2-27).

A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the XC4000 device keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the INIT input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output.

Using an open-collector or open-drain driver to hold $\overline{INIT}$ Low before the beginning of configuration, causes the LCA device to wait after having completed the configuration memory clear operation. When $\overline{INIT}$ is no longer held Low externally, the device determines its configuration mode by capturing its status inputs, and is ready to start the configuration process. A master device waits an additional max 250 µs to make sure that all slaves in the potential daisy-chain have seen $\overline{INIT}$ being High.

Master Parallel Mode Programming Switching Characteristics



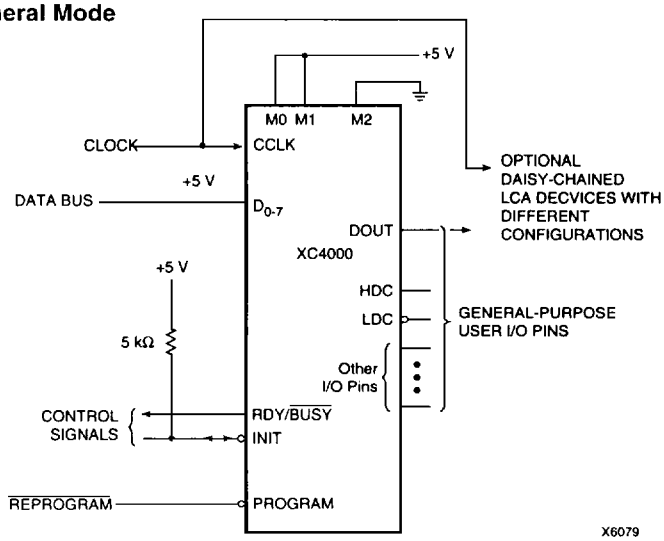
	Description	Symbol		Min	Max	Units
RCLK	Delay to Address valid	1	T_{RAC}	0	200	ns
	Data setup time	2	T_{DRC}	60		ns
	Data hold time	3	T_{RCD}	0		ns

Notes: 1. At power-up, V_{CC} must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration using $\overline{PROGRAM}$ until V_{CC} is valid.

2. Configuration can be delayed by holding $\overline{INIT}$ Low with or until after the $\overline{INIT}$ of all daisy-chain slave mode devices is High.
3. The first Data byte is loaded and CCLK starts at the end of the first $\overline{RCLK}$ active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed: EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

Synchronous Peripheral Mode



Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the LCA device(s). The first byte of parallel configuration data must be available at the D inputs of the lead LCA device a short set-up time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge. The same CCLK edge that accepts data, also causes the RDY/BUSY output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes.

The lead LCA device serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next LCA device in the daisy-chain accepts data on the subsequent rising CCLK edge. In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

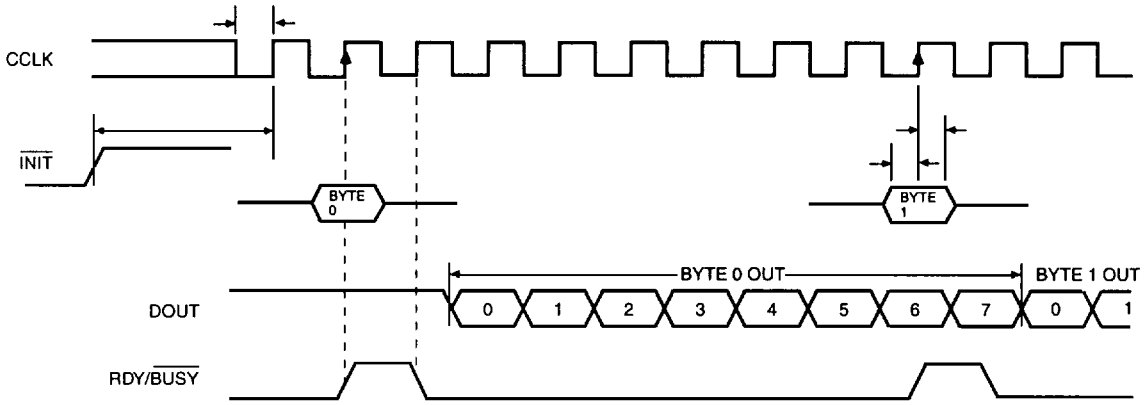
How to Delay Configuration After Power-Up

There are two methods to delay configuration after power-up: Put a logic Low on the $\overline{\text{PROGRAM}}$ input, or pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See also Figure 20 on page 2-27).

A Low on the $\overline{\text{PROGRAM}}$ input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as $\overline{\text{PROGRAM}}$ is Low, the XC4000 device keeps clearing its configuration memory. When $\overline{\text{PROGRAM}}$ goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the INIT input is not externally held Low. Note that a Low on the $\overline{\text{PROGRAM}}$ input automatically forces a Low on the $\overline{\text{INIT}}$ output.

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of configuration, causes the LCA device to wait after having completed the configuration memory clear operation. When $\overline{\text{INIT}}$ is no longer held Low externally, the device determines its configuration mode by capturing its status inputs, and is ready to start the configuration process. A master device waits an additional max 250 µs to make sure that all slaves in the potential daisy-chain have seen $\overline{\text{INIT}}$ being High.

Synchronous Peripheral Mode Programming Switching Characteristics



X6096

	Description	Symbol		Min	Max	Units
CCLK	INIT (High) Setup time required	1	T_{IC}	5		µs
	D0-D7 Setup time required	2	T_{DC}	60		ns
	D0-D7 Hold time required	3	T_{CD}	0		ns
	CCLK High time		T_{CCH}	50		ns
	CCLK Low time		T_{CCL}	60		ns
	CCLK Frequency		F_{CC}		8	MHz

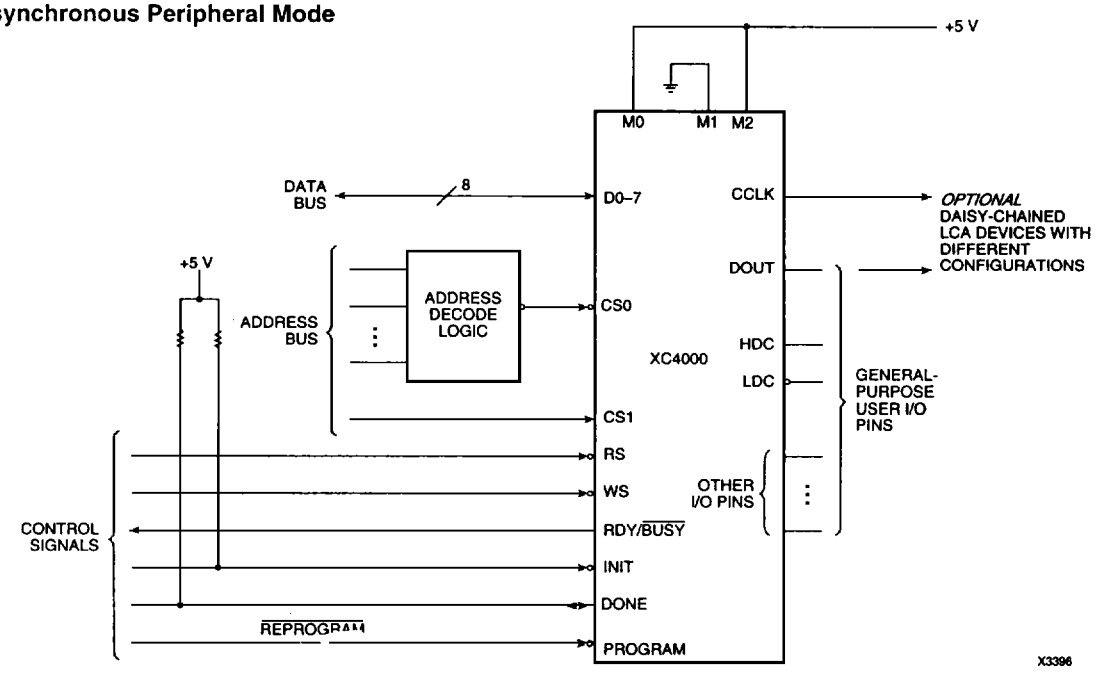
Notes: Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after INIT goes High. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.

The RDY/BUSY line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.

The pin name RDY/BUSY is a misnomer; in Synchronous Peripheral mode this is really an ACKNOWLEDGE signal.

Note that data starts to shift out serially on the DOUT pin 0.5 CLK periods after it was loaded in parallel. This obviously requires additional CCLK pulses after the last byte has been loaded.

Asynchronous Peripheral Mode



Write to LCA

Asynchronous Peripheral mode uses the trailing edge of the logic AND condition of the $\overline{CS0}$, CS1 and $\overline{WS}$ inputs to accept byte-wide data from a microprocessor bus. In the lead LCA device, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic. The lead LCA device presents the preamble data (and all data that overflows the lead device) on the DOUT pin.

The RDY/$\overline{BUSY}$ output from the lead LCA device acts as a handshake signal to the microprocessor. RDY/$\overline{BUSY}$ goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. The length of the $\overline{BUSY}$ signal depends on the activity in the UART. If the shift register had been empty when the new byte was received, the $\overline{BUSY}$ signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the $\overline{BUSY}$ signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered. The READY/$\overline{BUSY}$ handshake can be ignored if the delay from any one Write to the end of the next Write is guaranteed to be longer than 10 CCLK periods,i.e. longer than 20 µs.

Status Read

The logic AND condition of the $\overline{CS0}$, CS1and $\overline{RS}$ inputs puts the device status on the Data bus.

D7 = High indicates Ready
D7 - Low indicates Busy
D0 through D6 go unconditionally High

It is mandatory that the whole start-up sequence be started and completed by one byte-wide input. Otherwise, the pins used as Write Strobe or Chip Enable might become active outputs and inteffere with the final byte transfer. If this transfer does not occur, the start-up sequence will not be completed all the way to the finish (point F in Figure 21 on page 2-29). At worst, the internal reset will not be released; at best, Readback and Boundary Scan will be inhibited. The length-count value, as generated by MAKEPROM, is supposed to ensure that these problems never occur.

Although RDY/$\overline{BUSY}$ is brought out as a separate signal, microprocessors can more easily read this information on one of the data lines. For this purpose, D7 represents the RDY/$\overline{BUSY}$ status when $\overline{RS}$ is Low, $\overline{WS}$ is High, and the two chip select lines are both active.

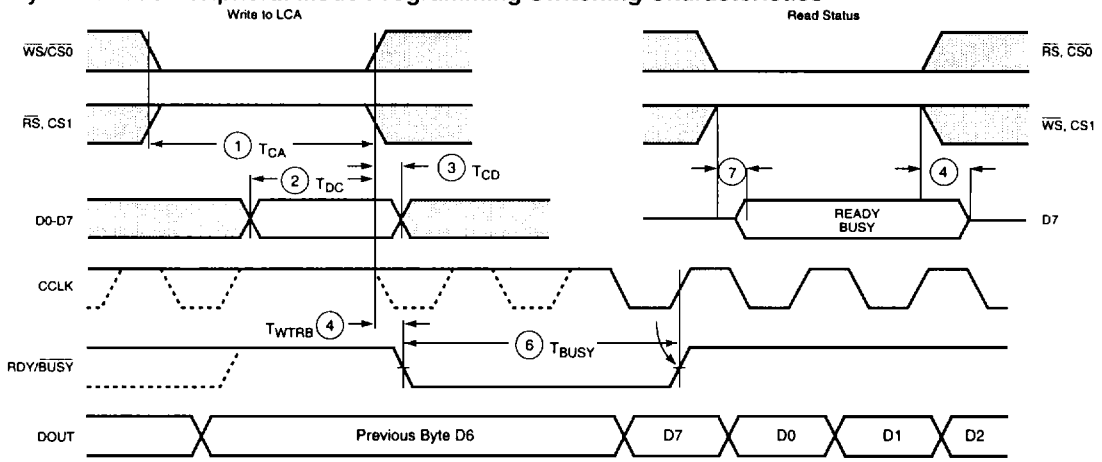
How to Delay Configuration After Power-Up

There are two methods to delay configuration after power-up: Put a logic Low on the $\overline{PROGRAM}$ input, or pull the bidirectional $\overline{INIT}$ pin Low, using an open-collector (open-drain) driver. (See also Figure 20 on page 2-27).

A Low on the PROGRAM input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as PROGRAM is Low, the XC4000 device keeps clearing its configuration memory. When PROGRAM goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the INIT input is not externally held Low. Note that a Low on the PROGRAM input automatically forces a Low on the INIT output.

Using an open-collector or open-drain driver to hold INIT Low before the beginning of configuration, causes the LCA device to wait after having completed the configuration memory clear operation. When INIT is no longer held Low externally, the device determines its configuration mode by capturing its status inputs, and is ready to start the configuration process. A master device waits an additional max 250 µs to make sure that all slaves in the potential daisy-chain have seen INIT being High.

Asynchronous Peripheral Mode Programming Switching Characteristics

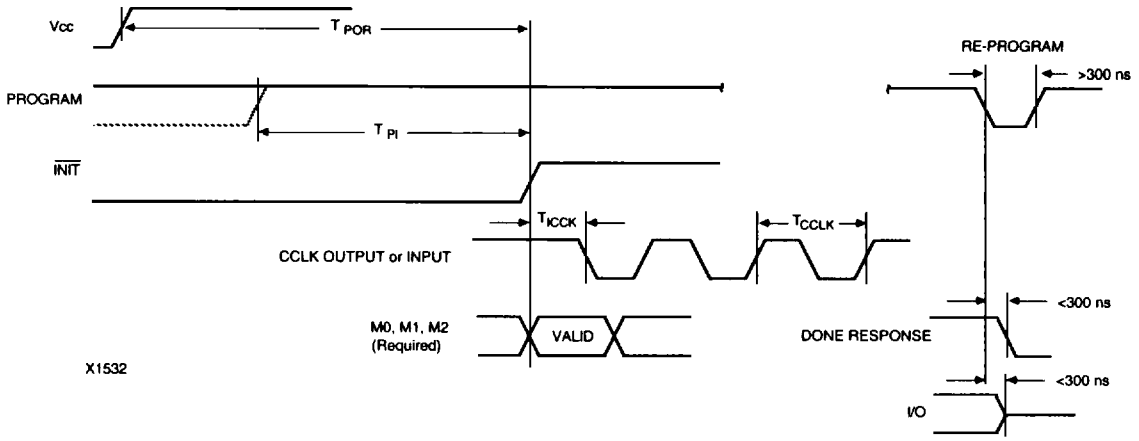


	Description		Symbol	Min	Max	Units
Write	Effective Write time required ($\overline{CS0}$, $\overline{WS}$ = Low, $\overline{RS}$, CS1 = High)	1	T_{CA}	100		ns
	DIN Setup time required	2	T_{DC}	60		ns
	DIN Hold time required	3	T_{CD}	0		ns
	RDY/$\overline{BUSY}$ delay after end of Write or Read	4	T_{WTRB}		60	ns
	RDY/BUSY active after begining of Read	7			60	ns
RDY	Earliest next $\overline{WS}$ after end of $\overline{BUSY}$	5	T_{RBWT}	0		ns
	$\overline{BUSY}$ Low output (Note 4)	6	T_{BUSY}	2	9	CCLK Periods

Notes:
1. Configuration must be delayed until the INIT of all LCA devices is High.
2. Time from end of $\overline{WS}$ to CCLK cycle for the new byte of data depends on completion of previous byte processing and the phase of the internal timing generator for CCLK.
3. CCLK and DOUT timing is tested in slave mode.
4. T_{BUSY} indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest T_{BUSY} occurs when a byte is loaded into an empty parallel-to-serial converter. The longest T_{BUSY} occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements:
Data need not be held beyond the rising edge of WS. BUSY will go active within 60 ns after the end of WS.
WS may be asserted immediately after the end of BUSY.

General LCA Switching Characteristics



Master Modes

		Symbol	Min	Max	Units
Power-On-Reset	M0 = High M0 = Low	T_{POR} T_{POR}	10 40	40 130	ms ms
Program Latency		T_{PI}	30	200	µs per CLB column
CCLK (output) Delay period (slow) period (fast)		T_{ICCK} T_{CCLK} T_{CCLK}	40 640 100	250 2000 250	µs ns ns

Slave and Peripheral Modes

	Symbol	Min	Max	Units
Power-On-Reset	T_{POR}	10	33	ms
Program Latency	T_{PI}	30	200	µs per CLB column
CCLK (input) Delay (required) period (required)	T_{ICCK} T_{CCLK}	4 100		µs ns

Note: At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less than 25 ms, otherwise delay configuration using PROGRAM until V_{CC} is valid.

Pin Functions During Configuration

CONFIGURATION MODE: <M2:M1:M0>						
SLAVE <1:1:1>	MASTER-SER <0:0:0>	SYN.PERIPH <0:1:1>	ASYN.PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	USER OPERATION
				A16	A16	PGI-I/O
				A17	A17	I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
						SGI-I/O
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	(O)
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	(I)
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	(I)
						PGI-I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
• $\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	$\overline{\text{INIT}}$-$\overline{\text{ERROR}}$	I/O
						SGI-I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
						PGI-I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
			$\overline{\text{CS0}}$ (I)			I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
			$\overline{\text{RS}}$ (I)			I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
		$\overline{\text{RDY}}$/BUSY	$\overline{\text{RDY}}$/BUSY	$\overline{\text{RCLK}}$	$\overline{\text{RCLK}}$	I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	SGI-I/O
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK(O)	CCLK (O)	CCLK (I)
TDO	TDO	TDO	TDO	TDO	TDO	TDO-(O)
			$\overline{\text{WS}}$ (I)	A0	A0	I/O
				A1	A1	PGI-I/O
			CS1 (I)	A2	A2	I/O
				A3	A3	I/O
				A4	A4	I/O
				A5	A5	I/O
				A6	A6	I/O
				A7	A7	I/O
				A8	A8	I/O
				A9	A9	I/O
				A10	A10	I/O
				A11	A11	I/O
				A12	A12	I/O
				A13	A13	I/O
				A14	A14	I/O
				A15	A15	SGI-I/O
						ALL OTHERS

X6081

Represents a 50 kΩ to 100 kΩ pull-up before and during configuration

* INIT is an open-drain output during configuration

(I) Represents an input

Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50 kΩ to 100 kΩ pull-up resistor.

Pin Descriptions

Permanently Dedicated Pins

V_{CC}

Eight or more (depending on package type) connections to the nominal +5 V supply voltage. All must be connected.

GND

Eight or more (depending on package type) connections to ground. All must be connected.

CCLK

During configuration, Configuration Clock is an output of the LCA in Master modes or asynchronous Peripheral mode, but is an input to the LCA in Slave mode and Synchronous Peripheral mode.

After configuration, CCLK has a weak pull-up resistor and can be selected as Readback Clock.

DONE

This is a bidirectional signal, configurable with or without a pull-up resistor of 2 to 8 kΩ.

As an output, it indicates the completion of the configuration process. The configuration program determines the exact timing, the clock source for the Low-to-High transition, and enable of the pull-up resistor.

As an input, a Low level on DONE can be configured to delay the global logic initialization or the enabling of outputs

$\overline{\text{PROGRAM}}$

This is an active Low input that forces the LCA to clear its configuration memory.

When $\overline{\text{PROGRAM}}$ goes High, the LCA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$.

User I/O Pins that can have Special Functions

RDY/$\overline{\text{BUSY}}$

During peripheral modes, this pin indicates when it is appropriate to write another byte of data into the LCA device. The same status is also available on D7 in asynchronous peripheral mode, if a read operation is performed when the device is selected. After configuration, this is a user-programmable I/O pin.

$\overline{\text{RCLK}}$

During Master Parallel configuration, each change on the A0-15 outputs is preceded by a rising edge on $\overline{\text{RCLK}}$, a redundant output signal. After configuration, this is a user-programmable I/O pin.

M0, M1, M2

As Mode inputs, these pins are sampled before the start of configuration to determine the configuration mode to be used.

After configuration, M0 and M2 can be used as inputs, and M1 can be used as a 3-state output. These three pins have no associated input or output registers.

These pins can be user inputs or outputs only when called out by special schematic definitions.

TDO

If boundary scan is used, this is the Test Data Output.

If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed.

This pin can be user output only when called out by special schematic definitions.

TDI,TCK, TMS

If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively coming directly from the pads, bypassing theIOBs. These pins can also be used as inputs to the CLB logic after configuration is completed.

If the boundary scan option is not selected, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O.

Note:
The XC4000 families have no Powerdown control input; use the global 3-state net instead.
The XC4000 families have no dedicated Reset input. Any user I/O can be configured to drive the global Set/Reset net.

HDC

High During Configuration is driven High until configuration is completed. It is available as a control output indicating that configuration is not yet completed. After configuration, this is a user-programmable I/O pin.

LDC

Low During Configuration is driven Low until configuration. It is available as a control output indicating that configuration is not yet completed. After configuration, this is a user-programmable I/O pin.

$\overline{\text{INIT}}$

Before and during configuration, this is a bidirectional signal. An external pull-up resistor is recommended.

As an active-Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active-Low input, it can be used to hold the LCA device in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High.

During configuration, a Low on this output indicates that a configuration data error has occurred. After configuration, this is a user-programmable I/O pin.

PGCK1 - PGCK4

Four Primary Global Inputs each drive a dedicated internal global net with short delay and minimal skew. If not used for this purpose, any of these pins is a user-programmable I/O.

SGCK1 - SGCK4

Four Secondary Global Inputs can each drive a dedicated internal global net, that alternatively can also be driven from internal logic. If not used for this purpose, any of these pins is a user-programmable I/O pin.

$\overline{\text{CS0}}$, CS1, $\overline{\text{WS}}$, $\overline{\text{RS}}$

These four inputs are used in Peripheral mode. The chip is selected when $\overline{\text{CS0}}$ is Low and CS1 is High. While the chip is selected, a Low on Write Strobe ($\overline{\text{WS}}$) loads the data present on the D0 - D7 inputs into the internal data buffer; a Low on Read Strobe ($\overline{\text{RS}}$) changes D7 into a status output: High if Ready, Low if Busy, and D0...D6 are active Low. $\overline{\text{WS}}$ and $\overline{\text{RS}}$ should be mutually exclusive, but if both are Low simultaneously, the Write Strobe overrides. After configuration, these are user-programmable I/O pins.

A0 - A17

During Master Parallel mode, these 18 output pins address the configuration EPROM. After configuration, these are user-programmable I/O pins.

D0 - D7

During Master Parallel and Peripheral configuration modes, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.

DIN

During Slave Serial or Master Serial configuration modes, this is the serial configuration data input receiving data on the rising edge of CCLK.

During parallel configuration modes, this is the D0 input. After configuration, DIN is a user-programmable I/O pin.

DOUT

During configuration in any mode, this is the serial configuration data output that can drive the DIN of daisy-chained slave LCA devices. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. After configuration, DOUT is a user-programmable I/O pin.

Unrestricted User-Programmable I/O Pins

I/O

A pin that can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor that defines the logic level as High.

Before and during configuration, all outputs that are not used for the configuration process are 3-stated with a 50 kΩ to 100 kΩ pull-up resistor.

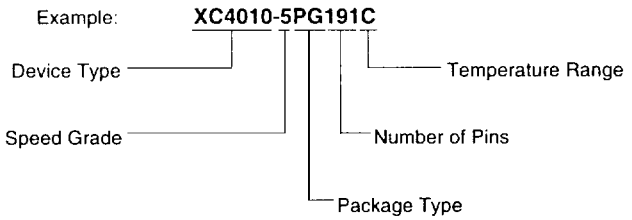
For a detailed description of the device architecture, see page 2-9 through 2-31.

For a detailed description of the configuration modes and their timing, see pages 2-32 through 2-55.

For detailed lists of package pinouts, see pages 2-57 through 2-67, 2-70, 2-81 through 2-85, and 2-100 through 2-101.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		84	100			120	144	156	160	164	191	196	208		223	225	240		299	304
TYPE		PLAST. PLCC	PLAST. PQFP	PLAST. VQFP	TOP BRAZED CQFP	CERAM. PGA	PLAST. TQFP	CERAM. PGA	PLAST. PQFP	TOP BRAZED CQFP	CERAM. PGA	TOP BRAZED CQFP	PLAST. PQFP	METAL PQFP	CERAM. PGA	PLAST. BGA	PLAST. PQFP	METAL PQFP	METAL PQFP	HI QUAD
CODE		PC84	PQ100	VQ100	CB100	PG120	TQ144	PG156	PQ160	CB164	PG191	CB196	PQ208	MQ208	PG223	BG225	PQ240	MQ240	PG299	HQ304
XC4003	-6	C I	C I			C I														
	-5	C	C			C														
	-4	C	C			C														
XC4005	-10							M B		M B										
	-6	C I	C I					C I M B	C I	M B			C I							
	-5	C I	C I					C I	C I				C I							
	-4	C	C					C	C				C							
XC4006	-6	C I						C I	C I				C I							
	-5	C I						C I	C I				C I							
	-4	C						C	C				C							
XC4008	-6	C I							C I		C I		C I	C I						
	-5	C I							C I		C I		C I	C I						
	-4	C							C		C		C	C						
XC4010	-10										M B	M B								
	-6	C I							C I		C I M B	M B	C I	C I		C I				
	-5	C I							C I		C I		C I	C I		C I				
	-4	C							C		C		C	C		C				
XC4010D	-6	C I							C I				C I			C I				
	-5	C I							C I				C I			C I				
	-4								C				C			C				
XC4013	-6								C I				C I	C I	C I (M B)	C I	C I	C I		
	-5								C I				C I	C I	C I	C I	C I	C I		
	-4								C				C	C	C	C	C	C		
XC4013D	-6								C I				C I			C I	C I			
	-5								C I				C I			C I	C I			
	-4								C				C			C	C			
XC4020	-6												(C I)		(C I)		(C I)		(C I)	
	-5												(C I)		(C I)		(C I)		(C I)	
	-4												(C)		(C)		(C)		(C)	
XC4025	-6														C I			C I	C I	C I
	-5														C I			C I	C I	C I
	-4														C			C	C	C
XC4002A	-6	C I	C I	C I		C I														
	-5	C	C	C		C														
	-4																			
XC4003A	-10				M B	M B														
	-6	C I	C I	C I	M B	C I M B														
	-5	C	C	C		C														
	-4	C	C	C		C														
XC4004A	-6	C I				C I	C I		C I											
	-5	C				C	C		C											
	-4																			
XC4005A	-6	C I					C I	C I	C I				C I							
	-5	C I					C I	C I	C I				C I							
	-4	C					C	C	C				C							
XC4003H	-6										C I		C I							
	-5										C		C							
XC4005H	-6														C I		C I	C I		
	-5														C		C	C		

C = Commercial = 0° to +85° C
B = MIL-STD-883C Class B
I = Industrial = -40° to +100° C
Parentheses indicate future product plans
M = Mil Temp = -55° to +125° C

XC4000
Logic Cell Array Family

Product Specifications

Features

- Third Generation Field-Programmable Gate Arrays
  - Abundant flip-flops
  - Flexible function generators
  - On-chip ultra-fast RAM
  - Dedicated high-speed carry-propagation circuit
  - Wide edge decoders (four per edge)
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution network
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and Interconnect
  - Low power consumption
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary-scan logic support
  - Programmable output slew rate (2 modes)
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per output
  - 24-mA sink current per output pair
- Configured by Loading Binary File
  - Unlimited reprogrammability
  - Six programming modes
- XACT Development System runs on '386/'486/ Pentium-type PC, Apollo, Sun-4, and Hewlett-Packard 700 series
  - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The XC4000 family of Field-Programmable Gate Arrays (FPGAs) provides the benefits of custom CMOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array.

The XC4000 family provides a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs).

XC4000 devices have generous routing resources to accommodate the most complex interconnect patterns. They are customized by loading configuration data into the internal memory cells. The FPGA can either actively read its configuration data out of external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA (slave and peripheral modes).

The XC4000 family is supported by powerful and sophisticated software, covering every aspect of design: from schematic entry, to simulation, to automatic block placement and routing of interconnects, and finally the creation of the configuration bit stream.

Since Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening the design and development cycle, but they also offer a cost-effective solution for production rates well beyond 1000 systems per month.

For a detailed description of the device features, architecture, configuration methods and pin descriptions, see pages 2-9 through 2-45.

Table 1. The XC4000 Family of Field-Programmable Gate Arrays

Device	XC4003	XC4005	XC4006	XC4008	XC4010/10D	XC4013/13D	XC4020	XC4025
Appr. Gate Count	3,000	5,000	6,000	8,000	10,000	13,000	20,000	25,000
CLB Matrix	10 x 10	14 x 14	16 x 16	18 x 18	20 x 20	24 x 24	28 x 28	32 x 32
Number of CLBs	100	196	256	324	400	576	784	1,024
Number of Flip-Flops	360	616	768	936	1,120	1,536	2,016	2,560
Max Decode Inputs (per side)	30	42	48	54	60	72	84	96
Max RAM Bits	3,200	6,272	8,192	10,368	12,800*	18,432	25,088	32,768
Number of IOBs	80	112	128	144	160	192	224	256

*XC4010D has no RAM

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+ 260	°C
T_J	Junction temperature	+ 150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to 100°C junction	4.5	5.5	V
	Supply voltage relative to GND Military –55°C to 125°C case	4.5	5.5	V
V_{IH}	High-level input voltage (XC4000 has TTL-like input thresholds)	2.0	V_{CC}	V
V_{IL}	Low-level input voltage (XC4000 has TTL-like input thresholds)	0	0.8	V
T_{IN}	Input signal transition time		250	ns

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (Note 1)		0.4	V
I_{CCO}	Quiescent LCA supply current (Note 2)		10	mA
I_{IL}	Leakage current	–10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.25	mA
I_{RLL}	Horizontal Long Line pull-up (when selected) @ logic Low	0.2	2.5	mA

Note: 1. With 50% of the outputs simultaneously sinking 12 mA.
2. With no output current loads, no active input or longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4003	9.0	8.0	5.0	ns
		XC4005	10.0	9.0	6.0	ns
		XC4006	11.0	10.0	7.0	ns
		XC4008	12.0	11.0	8.0	ns
		XC4010	13.0	12.0	9.0	ns
		XC4013	15.0	14.0	11.0	ns
		XC4025	21.0	19.0	17.0	ns
Full length, both pull-ups inputs from internal logic	T_{WAFL}	XC4003	12.0	11.0	7.0	ns
		XC4005	13.0	12.0	8.0	ns
		XC4006	14.0	13.0	9.0	ns
		XC4008	15.0	14.0	10.0	ns
		XC4010	16.0	15.0	11.0	ns
		XC4013	18.0	17.0	13.0	ns
		XC4025	24.0	23.0	20.0	ns
Half length, one pull-up inputs from IOB I-pins	T_{WAO}	XC4003	9.0	8.0	6.0	ns
		XC4005	10.0	9.0	7.0	ns
		XC4006	11.0	10.0	8.0	ns
		XC4008	12.0	11.0	9.0	ns
		XC4010	13.0	12.0	10.0	ns
		XC4013	15.0	14.0	12.0	ns
		XC4025	21.0	19.0	18.0	ns
Half length, one pull-up inputs from internal logic	T_{WAOL}	XC4003	12.0	11.0	8.0	ns
		XC4005	13.0	12.0	9.0	ns
		XC4006	14.0	13.0	10.0	ns
		XC4008	15.0	14.0	11.0	ns
		XC4010	16.0	15.0	12.0	ns
		XC4013	18.0	17.0	14.0	ns
		XC4025	24.0	23.0	21.0	ns

Note: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPF} or T_{OPS}), as listed on page 2-52.

PRELIMINARY

Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade	-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Global Signal Distribution						
From pad through **primary** buffer, to any clock K	T_{PG}	XC4003	7.8	5.8	5.1	ns
		XC4005	8.0	6.0	5.5	ns
		XC4006	8.2	6.2	5.7	ns
		XC4008	8.6	6.6	6.1	ns
		XC4010	9.0	7.0	6.5	ns
		XC4013	10.0	8.0	7.5	ns
		XC4025	17.0	15.0	14.5	ns
From pad through **secondary** buffer, to any clock K	T_{SG}	XC4003	8.8	6.8	6.3	ns
		XC4005	9.0	7.0	6.7	ns
		XC4006	9.2	7.2	6.9	ns
		XC4008	9.6	7.6	7.3	ns
		XC4010	10.0	8.0	7.7	ns
		XC4013	11.0	9.0	8.7	ns
		XC4025	18.0	16.0	15.7	ns

Horizontal Longline Switching Characteristic Guidelines

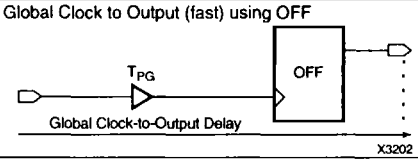
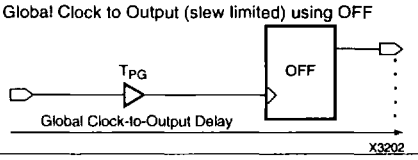
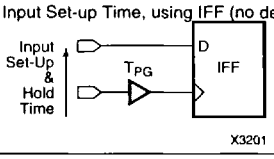
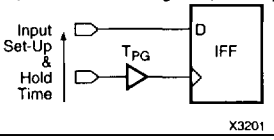
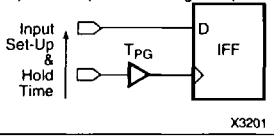
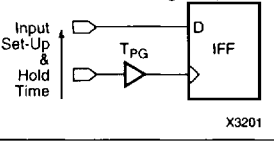
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade	-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (L.L.) I going High or Low to L.L. going High or Low, while T is Low, i.e. buffer is constantly active	T_{IO1}	XC4003	8.8	6.2	4.4	ns
		XC4005	10.0	7.0	5.5	ns
		XC4006	10.6	7.5	6.0	ns
		XC4008	11.1	8.0	6.5	ns
		XC4010	11.7	8.5	7.0	ns
		XC4013	13.0	9.5	7.5	ns
		XC4025	20.0	16.5	14.5	ns
I going Low to L.L. going from resistive pull-up High to active Low, (TBUF configured as open drain)	T_{IO2}	XC4003	9.3	6.7	5.0	ns
		XC4005	10.5	7.5	6.0	ns
		XC4006	11.1	8.0	6.5	ns
		XC4008	11.6	8.5	7.0	ns
		XC4010	12.2	9.0	7.5	ns
		XC4013	13.5	10.0	8.0	ns
		XC4025	23.5	20.0	18.0	ns
T going Low to L.L. going from resistive pull-up or floating High to active Low, (TBUF configured as open drain or active buffer with I = Low)	T_{ON}	XC4003	10.7	9.0	7.2	ns
		XC4005	12.0	10.0	8.0	ns
		XC4006	12.6	10.5	8.5	ns
		XC4008	13.2	11.0	9.0	ns
		XC4010	13.8	11.5	9.5	ns
		XC4013	15.1	12.6	11.1	ns
		XC4025	23.0	20.5	19.0	ns
T going High to TBUF going inactive, not driving L.L.	T_{OFF}	All devices	3.0	2.0	1.8	ns
T going High to L.L. going from Low to High, pulled up by a single resistor	T_{PUS}	XC4003	24.0	20.0	14.0	ns
		XC4005	26.0	22.0	16.0	ns
		XC4006	28.0	24.0	18.0	ns
		XC4008	30.0	26.0	20.0	ns
		XC4010	32.0	28.0	22.0	ns
		XC4013	36.0	32.0	26.0	ns
		XC4025	52.0	48.0	42.0	ns
T going High to L.L. going from Low to High, pulled up by two resistors	T_{PUF}	XC4003	11.6	9.0	7.0	ns
		XC4005	12.0	10.0	8.0	ns
		XC4006	13.0	11.0	9.0	ns
		XC4008	14.0	12.0	10.0	ns
		XC4010	15.0	13.0	11.0	ns
		XC4013	17.0	15.0	13.0	ns
		XC4025	24.0	22.0	20.0	ns

PRELIMINARY

Guaranteed Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between these two methods, the values listed below should be used, and the derived values must be ignored.

Description	Symbol	Device	-6	-5	-4	Units
Global Clock to Output (fast) using OFF 	T_{ICKOF}	XC4003	15.1	12.5	11.6	ns
		XC4005	15.5	13.0	12.0	ns
		XC4006	15.7	13.2	12.2	ns
	(Max)	XC4008	16.1	13.6	12.6	ns
		XC4010	16.5	14.0	13.0	ns
		XC4013	17.5	15.0	14.0	ns
		XC4025	25.5	22.0	21.0	ns
Global Clock to Output (slew limited) using OFF 	T_{ICKO}	XC4003	19.9	15.2	14.4	ns
		XC4005	20.5	16.0	15.0	ns
		XC4006	20.7	16.2	15.2	ns
	(Max)	XC4008	21.1	16.6	15.6	ns
		XC4010	21.5	17.0	16.0	ns
		XC4013	22.5	18.0	17.0	ns
		XC4025	29.5	25.0	24.0	ns
Input Set-up Time, using IFF (no delay) 	T_{PSUF}	XC4003	2.4	2.0	1.6	ns
		XC4005	2.0	1.5	1.2	ns
		XC4006	1.8	1.3	1.0	ns
	(Min)	XC4008	1.4	0.9	0.6	ns
		XC4010	1.0	0.5	0.2	ns
		XC4013	0.5	0	0	ns
		XC4025	0	0	0	ns
Input Hold time, using IFF (no delay) 	T_{PHF}	XC4003	5.1	4.0	4.0	ns
		XC4005	5.5	4.5	4.5	ns
		XC4006	5.7	4.7	4.7	ns
	(Min)	XC4008	6.1	5.1	5.1	ns
		XC4010	6.5	5.5	5.5	ns
		XC4013	7.5	6.5	6.5	ns
		XC4025	18.0	16.0	15.5	ns
Input Set-up Time, using IFF (with delay) 	T_{PSU}	XC4003	21.5	18.5	12.0	ns
		XC4005	21.0	18.0	12.0	ns
		XC4006	20.8	17.8	12.0	ns
	(Min)	XC4008	20.4	17.4	12.0	ns
		XC4010	20.0	17.0	12.0	ns
		XC4013	19.0	16.0	12.0	ns
		XC4025	18.0	15.0	12.0	ns
Input Hold Time, using IFF (with delay) 	T_{PH}	XC4003	0	0	0	ns
		XC4005	0	0	0	ns
		XC4006	0	0	0	ns
	(Min)	XC4008	0	0	0	ns
		XC4010	0	0	0	ns
		XC4013	0	0	0	ns
		XC4025	0	0	0	ns

Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). When testing fast outputs, only one output switches. When testing slew-rate limited outputs, half the number of outputs on one side of the device are switching. These parameter values are tested and guaranteed for worst-case conditions of supply voltage and temperature, and also with the most unfavorable clock polarity choice.

T_{PDLI} for -4 Speed Grade

Pad to I1, I2 via transparent latch, with delay	XC4003	17.6 ns
	XC4005	17.9 ns
	XC4006	18.0 ns
	XC4008	18.3 ns
	XC4010	18.6 ns
	XC4013	19.3 ns
	XC4025	23.5 ns

PRELIMINARY

See page 2-52

T_{PICKD} for -4 Speed Grade

Input set-up time pad to clock (IK) with delay	XC4003	15.6 ns
	XC4005	15.9 ns
	XC4006	16.0 ns
	XC4008	16.3 ns
	XC4010	16.6 ns
	XC4013	17.3 ns
	XC4025	22.5 ns

X6082

IOB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade		-6		-5		-4		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input								
Propagation Delays								
Pad to I1, I2	T_{PID}		4.0		3.0		2.8	ns
Pad to I1, I2, via transparent latch (no delay)	T_{PLI}		8.0		7.0		6.0	ns
Pad to I1, I2, via transparent latch (with delay)	T_{PDLI}		26.0		24.0		**	ns
Clock (IK) toI1, I2, (flip-flop)	T_{IKRI}		8.0		7.0		6.0	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}		8.0		7.0		6.0	ns
Set-up Time (Note 3)								
Pad to Clock (IK), no delay	T_{PICK}	7.0		6.0		4.0		ns
Pad to Clock (IK) with delay	T_{PICKD}	25.0		24.0		**		ns
Hold Time (Note 3)								
Pad to Clock (IK), no delay	T_{IKPI}	1.0		1.0		1.0		ns
Pad to Clock (IK) with delay	T_{IKPID}	neg		neg		neg		ns
Output								
Propagation Delays								
Clock (OK) to Pad (fast)	T_{OKPOF}		7.5		7.0		6.5	ns
same (slew rate limited)	T_{OKPOS}		11.5		10.0		9.5	ns
Output (O) to Pad (fast)	T_{OPF}		9.0		7.0		5.5	ns
same (slew-rate limited)	T_{OPS}		13.0		10.0		8.5	ns
3-state to Pad begin hi-Z (slew-rate independent)	T_{TSHZ}		9.0		7.0		6.5	ns
3-state to Pad active and valid (fast)	T_{TSONF}		13.0		10.0		9.5	ns
same (slew -rate limited)	T_{TSONS}		17.0		13.0		12.5	ns
Set-up and Hold Times								
Output (O) to clock (OK) set-up time	T_{OOK}	8.0		6.0		5.5		ns
Output (O) to clock (OK) hold time	T_{OKO}	0		0		0		ns
Clock								
Clock High or Low time	T_{CH}/T_{CL}	5.0		4.5		4.0		ns
Global Set/Reset								
Delay from GSR net through Q to I1, I2	T_{RRI}		14.5		13.5		13.5	ns
Delay from GSR net to Pad	T_{RPO}		18.0		17.0		14.0	ns
GSR width*	T_{MRW}	21.0		18.0		18.0		ns

* Timing is based on the XC4005. For other devices see XACT timing calculator.
** See preceding page

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). **Slew rate limited** output rise/fall times are approximately two times longer than **fast** output rise/fall times. For the effect of capacitive loads on ground bounce, see pages 8-8 through 8-10.

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor or alternatively configured as a driven output or be driven from an external source.

3. Input pad setup times and hold times are specified with respect to the internal clock (IK). To calculate system setup time, subtract clock delay (clock pad to IK) from the specified input pad setup time value, but do not subtract below zero. Negative hold time means that the delay in the input data is adequate for the **external system hold time** to be zero, provided the input clock uses the Global signal distribution from pad to IK.

CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade		-6		-5		-4		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		6.0		4.5		4.0	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		8.0		7.0		6.0	ns
C inputs via H' to X/Y outputs	T_{HHO}		7.0		5.0		4.5	ns
CLB Fast Carry Logic								
Operand inputs (F1,F2,G1,G4) to COUT	T_{OPCY}		7.0		5.5		5.0	ns
Add/Subtract input (F3) to COUT	T_{ASCY}		8.0		6.0		5.5	ns
Initialization inputs (F1,F3) to COUT	T_{INCY}		6.0		4.0		3.5	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		8.0		6.0		5.5	ns
C_{IN} to C_{OUT}, bypass function generators.	T_{BYP}		2.0		1.5		1.5	ns
Sequential Delays								
Clock K to outputs Q	T_{CKO}		5.0		3.0		3.0	ns
Set-up Time before Clock K								
F/G inputs	T_{ICK}	6.0		4.5		4.5		ns
F/G inputs via H'	T_{IHCK}	8.0		6.0		6.0		ns
C inputs via H1	T_{HHCK}	7.0		5.0		5.0		ns
C inputs via DIN	T_{DICK}	4.0		3.0		3.0		ns
C inputs via EC	T_{ECCK}	7.0		4.0		3.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	6.0		4.5		4.0		ns
C_{IN} input via F'/G'	T_{CCK}	8.0		6.0		5.5		ns
C_{IN} input via F'/G' and H'	T_{CHCK}	10.0		7.5		7.3		ns
Hold Time after Clock K								
F/G inputs	T_{CKI}	0		0		0		ns
F/G inputs via H'	T_{CKIH}	0		0		0		ns
C inputs via H1	T_{CKHH}	0		0		0		ns
C inputs via DIN	T_{CKDI}	0		0		0		ns
C inputs via EC	T_{CKEC}	0		0		0		ns
C inputs via S/R, going Low (inactive)	T_{CKR}	0		0		0		ns
Clock								
Clock High time	T_{CH}	5.0		4.5		4.0		ns
Clock Low time	T_{CL}	5.0		4.5		4.0		ns
Set/Reset Direct								
Width (High)	T_{RPW}	5.0		4.0		4.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		9.0		8.0		7.0	ns
Master Set/Reset*								
Width (High or Low)	T_{MRW}	21.0		18.0		18.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}		33.0		31.0		28.0	ns

* Timing is based on the XC4005. For other devices see XACT timing calculator.

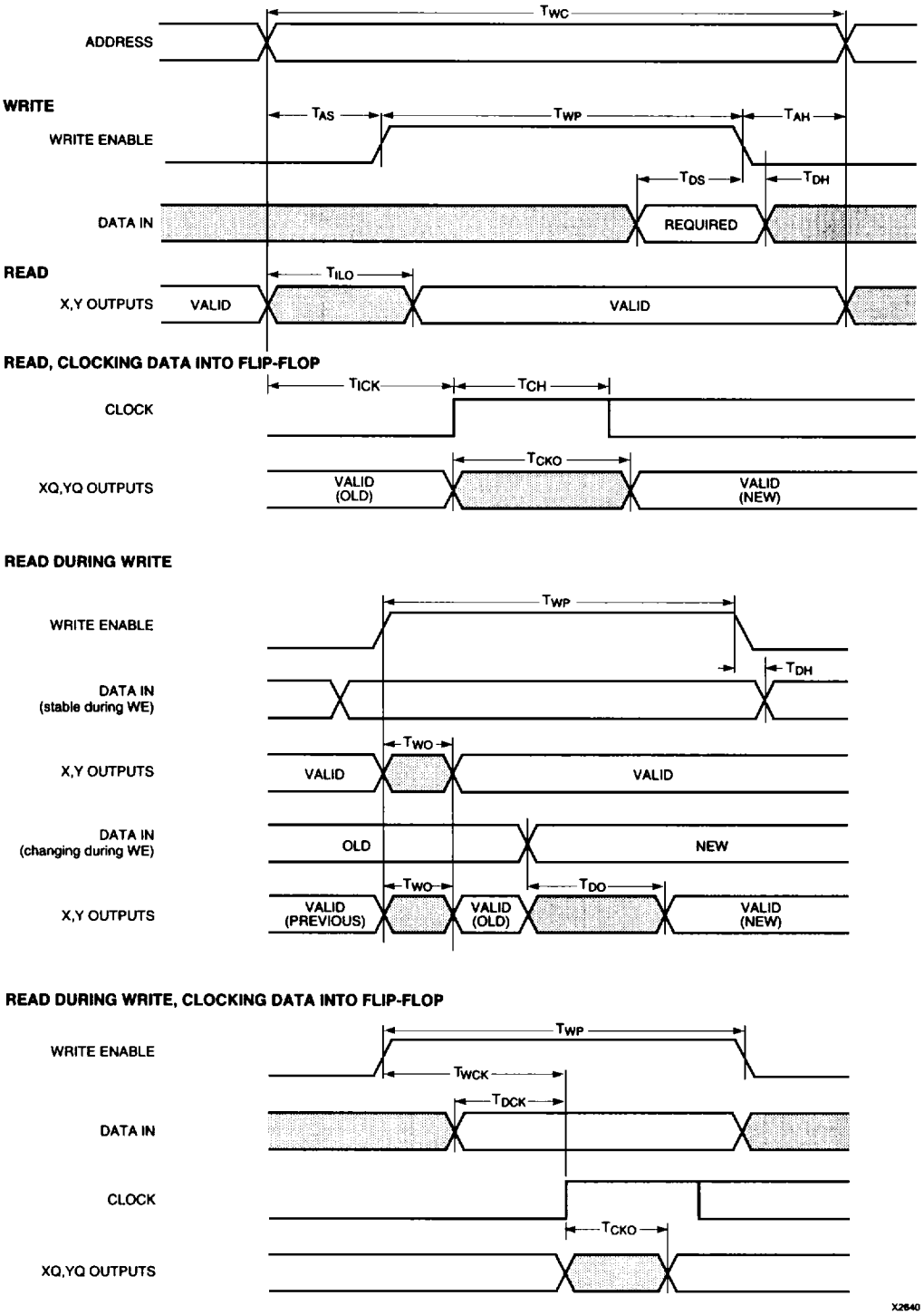
CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

CLB RAM Option	Speed Grade		-6		-5		-4		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Operation									
Address write cycle time	16 x 2	T_{WC}	9.0		8.0		8.0		ns
	32 x 1	T_{WCT}	9.0		8.0		8.0		ns
Write Enable pulse width (High)	16 x 2	T_{WP}	5.0		4.0		4.0		ns
	32 x 1	T_{WPT}	5.0		4.0		4.0		ns
Address set-up time before beginning of WE	16 x 2	T_{AS}	2.0		2.0		2.0		ns
	32 x 1	T_{AST}	2.0		2.0		2.0		ns
Address hold time after end of WE	16 x 2	T_{AH}	2.0		2.0		2.0		ns
	32 x 1	T_{AHT}	2.0		2.0		2.0		ns
DIN set-up time before end of WE	16 x 2	T_{DS}	4.0		4.0		4.0		ns
	32 x 1	T_{DST}	5.0		5.0		5.0		ns
DIN hold time after end of WE	both	T_{DHT}	2.0		2.0		2.0		ns
Read Operation									
Address read cycle time	16 x 2	T_{RC}	7.0		5.5		5.0		ns
	32 x 1	T_{RCT}	10.0		7.5		7.0		ns
Data valid after address change	16 x 2	T_{ILO}		6.0		4.5		4.0	ns
(no Write Enable)	32 x 1	T_{IHO}		8.0		7.0		6.0	ns
Read Operation, Clocking Data into Flip-Flop									
Address setup time before clock K	16 x 2	T_{ICK}	6.0		4.5		4.5		ns
	32 x 1	T_{IHCK}	8.0		6.0		6.0		ns
Read During Write									
Data valid after WE going active	16 x 2	T_{WO}		12.0		10.0		9.0	ns
(DIN stable before WE)	32 x 1	T_{WOT}		15.0		12.0		11.0	ns
Data valid after DIN	16 x 2	T_{DO}		11.0		9.0		8.5	ns
(DIN change during WE)	32 x 1	T_{DOT}		14.0		11.0		11.0	ns
Read During Write, Clocking Data into Flip-Flop									
WE setup time before clock K	16 x 2	T_{WCK}	12.0		10.0		9.5		ns
	32 x 1	T_{WCKT}	15.0		12.0		11.5		ns
Data setup time before clock K	16 x 2	T_{DCK}	11.0		9.0		9.0		ns
	32 x 1	T_{DCKT}	14.0		11.0		11.0		ns

Note: Timing for the 16 x 1 RAM option is identical to 16 x 2 RAM timing

CLB RAM Timing Characteristics



XC4003 Pinouts

Pin Description	PC84	PQ100	PG120	Bound Scan
VCC	2	92	G3	–
I/O (A8)	3	93	G1	32
I/O (A9)	4	94	F1	35
I/O	–	95	E1	38
I/O	–	96	F2	41
I/O (A10)	5	97	F3	44
I/O (A11)	6	98	D1	47
–	–	–	E2*	–
I/O (A12)	7	99	C1	50
I/O (A13)	8	100	D2	53
–	–	–	E3*	–
–	–	–	B1*	–
I/O (A14)	9	1	C2	56
SGCK1 (A15,I/O)	10	2	D3	59
VCC	11	3	C3	–
GND	12	4	C4	–
PGCK1 (A16, I/O)	13	5	B2	62
I/O (A17)	14	6	B3	65
–	–	–	A1*	–
–	–	–	A2*	–
I/O (TDI)	15	7	C5	68
I/O (TCK)	16	8	B4	71
–	–	–	A3*	–
I/O (TMS)	17	9	B5	74
I/O	18	10	A4	77
I/O	–	–	C6	80
I/O	–	11	A5	83
I/O	19	12	B6	86
I/O	20	13	A6	89
GND	21	14	B7	–
VCC	22	15	C7	–
I/O	23	16	A7	92
I/O	24	17	A8	95
I/O	–	18	A9	98
I/O	–	–	B8	101
I/O	25	19	C8	104
I/O	26	20	A10	107
I/O	27	21	B9	110
I/O	–	22	A11	113
–	–	–	B10*	–
I/O	28	23	C9	116
SGCK2 (I/O)	29	24	A12	119
O (M1)	30	25	B11	122
GND	31	26	C10	–
I (M0)	32	27	C11	125†
VCC	33	28	D11	–
I (M2)	34	29	B12	126†
PGCK2 (I/O)	35	30	C12	127
I/O (HDC)	36	31	A13	130
–	–	–	B13*	–
–	–	–	E11*	–
I/O	–	32	D12	133
I/O (LDC)	37	33	C13	136
I/O	38	34	E12	139
I/O	39	35	D13	142
I/O	–	36	F11	145
I/O	–	37	E13	148
I/O	40	38	F12	151
I/O (ERR, INIT)	41	39	F13	154
VCC	42	40	G12	–

Pin Description	PC84	PQ100	PG120	Bound Scan
GND	43	41	G11	–
I/O	44	42	G13	157
I/O	45	43	H13	160
I/O	–	44	J13	163
I/O	–	45	H12	166
I/O	46	46	H11	169
I/O	47	47	K13	172
I/O	48	48	J12	175
I/O	49	49	L13	178
–	–	–	K12*	–
–	–	–	J11*	–
I/O	50	50	M13	181
SGCK3 (I/O)	51	51	L12	184
GND	52	52	K11	–
DONE	53	53	L11	–
VCC	54	54	L10	–
PROG	55	55	M12	–
I/O (D7)	56	56	M11	187
PGCK3 (I/O)	57	57	N13	190
–	–	–	N12*	–
–	–	–	L9*	–
I/O (D6)	58	58	M10	193
I/O	–	59	N11	196
I/O (D5)	59	60	M9	199
I/O (CS0)	60	61	N10	202
I/O	–	62	L8	205
I/O	–	63	N9	208
I/O (D4)	61	64	M8	211
I/O	62	65	N8	214
VCC	63	66	M7	–
GND	64	67	L7	–
I/O (D3)	65	68	N7	217
I/O (RS)	66	69	N6	220
I/O	–	70	N5	223
I/O	–	–	M6	226
I/O (D2)	67	71	L6	229
I/O	68	72	N4	232
I/O (D1)	69	73	M5	235
I/O (RCLK-BUSY/RDY)	70	74	N3	238
–	–	–	M4*	–
–	–	–	L5*	–
I/O (D0, DIN)	71	75	N2	241
SGCK4 (DOUT, I/O)	72	76	M3	244
CCLK	73	77	L4	–
VCC	74	78	L3	–
O (TDO)	75	79	M2	–
GND	76	80	K3	–
I/O (A0, WS)	77	81	L2	2
PGCK4 (A1, I/O)	78	82	N1	5
–	–	–	M1*	–
–	–	–	J3*	–
I/O (CS1, A2)	79	83	K2	8
I/O (A3)	80	84	L1	11
I/O (A4)	81	85	J2	14
I/O (A5)	82	86	K1	17
I/O	–	87	H3	20
I/O	–	88	J1	23
I/O (A6)	83	89	H2	26
I/O (A7)	84	90	H1	29
GND	1	91	G2	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 247 = BSCANT.UPD

XC4005 Pinouts

Pin Description	PC 84	PQ 100	PQ 160	PQ 208	PG 156	Bound Scan
VCC	2	92	142	183	H3	-
I/O (A8)	3	93	143	184	H1	44
I/O (A9)	4	94	144	185	G1	47
I/O	-	95	145	186	G2	50
I/O	-	96	146	187	G3	53
-	-	-	-	188*	-	-
-	-	-	-	189*	-	-
I/O (A10)	5	97	147	190	F1	56
I/O (A11)	6	98	148	191	F2	59
I/O	-	-	149	192	E1	62
I/O	-	-	150	193	E2	65
GND	-	-	151	194	F3	-
-	-	-	-	195*	-	-
-	-	-	-	196*	-	-
-	-	-	152*	197*	D1*	-
-	-	-	153*	198*	D2*	-
I/O (A12)	7	99	154	199	E3	68
I/O (A13)	8	100	155	200	C1	71
-	-	-	-	-	-	-
I/O	-	-	156	201	C2	74
I/O	-	-	157	202	D3	77
I/O (A14)	9	1	158	203	B1	80
SGCK1 (A15, I/O)	10	2	159	204	B2	83
VCC	11	3	160	205	C3	-
-	-	-	-	206*	-	-
-	-	-	-	207*	-	-
-	-	-	-	208*	-	-
-	-	-	-	1*	-	-
GND	12	4	1	2	C4	-
-	-	-	-	3*	-	-
PGCK1 (A16, I/O)	13	5	2	4	B3	86
I/O (A17)	14	6	3	5	A1	89
I/O	-	-	4	6	A2	92
I/O	-	-	5	7	C5	95
-	-	-	-	-	-	-
I/O (TDI)	15	7	6	8	B4	98
I/O (TCK)	16	8	7	9	A3	101
-	-	-	8*	10*	A4*	-
-	-	-	9*	11*	-	-
-	-	-	-	12*	-	-
-	-	-	-	13*	-	-
GND	-	-	10	14	C6	-
I/O	-	-	11	15	B5	104
I/O	-	-	12	16	B6	107
I/O (TMS)	17	9	13	17	A5	110
I/O	18	10	14	18	C7	113
-	-	-	-	19*	-	-
-	-	-	-	20*	-	-
I/O	-	-	15	21	B7	116
I/O	-	11	16	22	A6	119
I/O	19	12	17	23	A7	122
I/O	20	13	18	24	A8	125
GND	21	14	19	25	C8	-
VCC	22	15	20	26	B8	-
I/O	23	16	21	27	C9	128
I/O	24	17	22	28	B9	131
I/O	-	18	23	29	A9	134
I/O	-	-	24	30	B10	137
-	-	-	-	31*	-	-
-	-	-	-	32*	-	-
I/O	25	19	25	33	C10	140
I/O	26	20	26	34	A10	143
I/O	-	-	27	35	A11	146
I/O	-	-	28	36	B11	149
GND	-	-	29	37	C11	-
-	-	-	-	38*	-	-
-	-	-	-	39*	-	-
-	-	-	30*	40*	A12*	-
-	-	-	31*	41*	-	-
I/O	27	21	32	42	B12	152
I/O	-	22	33	43	A13	155
I/O	-	-	34	44	A14	158

Pin Description	PC 84	PQ 100	PQ 160	PQ 208	PG 156	Bound Scan
I/O	-	-	35	45	C12	161
-	-	-	-	-	-	-
I/O	28	23	36	46	B13	164
SGCK2 (I/O)	29	24	37	47	B14	167
O (M1)	30	25	38	48	A15	170
GND	31	26	39	49	C13	-
I (M0)	32	27	40	50	A16	173†
-	-	-	-	51*	-	-
-	-	-	-	52*	-	-
-	-	-	-	53*	-	-
-	-	-	-	54*	-	-
VCC	33	28	41	55	C14	-
I (M2)	34	29	42	56	B15	174†
PGCK2 (I/O)	35	30	43	57	B16	175
I/O (HDC)	36	31	44	58	D14	178
I/O	-	-	45	59	C15	181
-	-	-	-	-	-	-
I/O	-	-	46	60	D15	184
I/O	-	32	47	61	E14	187
I/O ($\overline{LDC}$)	37	33	48	62	C16	190
-	-	-	49*	63*	E15*	-
-	-	-	50*	64*	D16*	-
-	-	-	-	65*	-	-
-	-	-	-	66*	-	-
GND	-	-	51	67	F14	-
I/O	-	-	52	68	F15	193
I/O	-	-	53	69	E16	196
I/O	38	34	54	70	F16	199
I/O	39	35	55	71	G14	202
-	-	-	-	72*	-	-
-	-	-	-	73*	-	-
I/O	-	36	56	74	G15	205
I/O	-	37	57	75	G16	208
I/O	40	38	58	76	H16	211
I/O ($\overline{ERR}$, $\overline{INIT}$)	41	39	59	77	H15	214
VCC	42	40	60	78	H14	-
GND	43	41	61	79	J14	-
I/O	44	42	62	80	J15	217
I/O	45	43	63	81	J16	220
I/O	-	44	64	82	K16	223
I/O	-	45	65	83	K15	226
-	-	-	-	84*	-	-
-	-	-	-	85*	-	-
I/O	46	46	66	86	K14	229
I/O	47	47	67	87	L16	232
I/O	-	-	68	88	M16	235
I/O	-	-	69	89	L15	238
GND	-	-	70	90	L14	-
-	-	-	-	91*	-	-
-	-	-	-	92*	-	-
-	-	-	71*	93*	N16*	-
-	-	-	72*	94*	M15*	-
I/O	48	48	73	95	P16	241
I/O	49	49	74	96	M14	244
I/O	-	-	75	97	N15	247
I/O	-	-	76	98	P15	250
I/O	50	50	77	99	N14	253
SGCK3 (I/O)	51	51	78	100	R16	256
GND	52	52	79	101	P14	-
-	-	-	-	102*	-	-
DONE	53	53	80	103	R15	-
-	-	-	-	104*	-	-
-	-	-	-	105*	-	-
VCC	54	54	81	106	P13	-
-	-	-	-	107*	-	-
$\overline{PROG}$	55	55	82	108	R14	-
I/O (D7)	56	56	83	109	T16	259
PGCK3 (I/O)	57	57	84	110	T15	262
I/O	-	-	85	111	R13	265
-	-	-	-	-	-	-
I/O	-	-	86	112	P12	268
I/O (D6)	58	58	87	113	T14	271

Pin Description	PC 84	PQ 100	PQ 160	PQ 208	PG 156	Bound Scan
I/O	-	59	88	114	T13	274
-	-	-	89*	115*	R12*	-
-	-	-	89*	115*	R12*	-
-	-	-	90†	116*	T12*	-
-	-	-	-	117*	-	-
-	-	-	-	118*	-	-
GND	-	-	91	119	P11	-
I/O	-	-	92	120	R11	277
I/O	-	-	93	121	T11	280
I/O (D5)	59	60	94	122	T10	283
I/O ($\overline{CS0}$)	60	61	95	123	P10	286
-	-	-	-	124*	-	-
-	-	-	-	125*	-	-
I/O	-	62	96	126	R10	289
I/O	-	63	97	127	T9	292
I/O (D4)	61	64	98	128	R9	295
I/O	62	65	99	129	P9	298
VCC	63	66	100	130	R8	-
GND	64	67	101	131	P8	-
I/O (D3)	65	68	102	132	T8	301
I/O ($\overline{RS}$)	66	69	103	133	T7	304
I/O	-	70	104	134	T6	307
I/O	-	-	105	135	R7	310
-	-	-	-	136*	-	-
-	-	-	-	137*	-	-
I/O (D2)	67	71	106	138	P7	313
I/O	68	72	107	139	T5	316
I/O	-	-	108	140	R6	319
I/O	-	-	109	141	T4	322
GND	-	-	110	142	P6	-
-	-	-	-	143*	-	-
-	-	-	-	144*	-	-
-	-	-	111*	145*	R5*	-
-	-	-	112*	146*	-	-
I/O (D1)	69	73	113	147	T3	325
I/O (RCLK-$\overline{BUSY}$/RDY)	70	74	114	148	P5	328
I/O	-	-	115	149	R4	331
-	-	-	-	-	-	-
I/O	-	-	116	150	R3	334
I/O (D0, DIN)	71	75	117	151	P4	337
SGCK4 (DOUT, I/O)	72	76	118	152	T2	340
CCLK	73	77	119	153	R2	-
VCC	74	78	120	154	P3	-
-	-	-	-	155*	-	-
-	-	-	-	156*	-	-
-	-	-	-	157*	-	-
-	-	-	-	158*	-	-
O (TDO)	75	79	121	159	T1	-
GND	76	80	122	160	N3	-
I/O (A0, $\overline{WS}$)	77	81	123	161	R1	2
PGCK4 (A1, I/O)	78	82	124	162	P2	5
I/O	-	-	125	163	N2	8
-	-	-	-	-	-	-
I/O	-	-	126	164	M3	11
I/O ($\overline{CS1}$, A2)	79	83	127	165	P1	14
I/O (A3)	80	84	128	166	N1	17
-	-	-	129*	167*	M2*	-
-	-	-	130*	168*	M1*	-
-	-	-	-	169*	-	-
-	-	-	-	170*	-	-
GND	-	-	131	171	L3	-
I/O	-	-	132	172	L2	20
I/O	-	-	133	173	L1	23
I/O (A4)	81	85	134	174	K3	26
I/O (A5)	82	86	135	175	K2	29
-	-	-	-	176*	-	-
-	-	-	136*	177*	-	-
I/O	-	87	137	178	K1	32
I/O	-	88	138	179	J1	35
I/O (A6)	83	89	139	180	J2	38
I/O (A7)	84	90	140	181	J3	41
GND	1	91	141	182	H2	-

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 343 = BSCANT.UPD

XC4006 Pinouts

Pin Description	PC 84	PG 156	PQ 160	PQ 208	Boundary Scan Order
VCC	2	H3	142	183	-
I/O (A8)	3	H1	143	184	50
I/O (A9)	4	G1	144	185	53
I/O	-	G2	145	186	56
I/O	-	G3	146	187	59
-	-	-	-	188*	-
-	-	-	-	189*	-
I/O (A10)	5	F1	147	190	62
I/O (A11)	6	F2	148	191	65
I/O	-	E1	149	192	68
I/O	-	E2	150	193	71
GND	-	F3	151	194	-
-	-	-	-	195*	-
-	-	-	-	196*	-
I/O	-	D1	152	197	74
I/O	-	D2	153	198	77
I/O (A12)	7	E3	154	199	80
I/O (A13)	8	C1	155	200	83
I/O	-	C2	156	201	86
I/O	-	D3	157	202	89
I/O (A14)	9	B1	158	203	92
SGCK1 (A15, I/O)	10	B2	159	204	95
VCC	11	C3	160	205	-
-	-	-	-	206*	-
-	-	-	-	207*	-
-	-	-	-	208*	-
-	-	-	-	1*	-
GND	12	C4	1	2	-
-	-	-	-	3*	-
PGCK1 (A16, I/O)	13	B3	2	4	98
I/O (A17)	14	A1	3	5	101
I/O	-	A2	4	6	104
I/O	-	C5	5	7	107
I/O (TDI)	15	B4	6	8	110
I/O (TCK)	16	A3	7	9	113
I/O	-	A4	8	10	116
I/O	-	-	9	11	119
-	-	-	-	12*	-
-	-	-	-	13*	-
GND	-	C6	10	14	-
I/O	-	B5	11	15	122
I/O	-	B6	12	16	125
I/O (TMS)	17	A5	13	17	128
I/O	18	C7	14	18	131
-	-	-	-	19*	-
-	-	-	-	20*	-
I/O	-	B7	15	21	134
I/O	-	A6	16	22	137
I/O	19	A7	17	23	140
I/O	20	A8	18	24	143
GND	21	C8	19	25	-
VCC	22	B8	20	26	-

Pin Description	PC 84	PG 156	PQ 160	PQ 208	Boundary Scan Order
I/O	23	C9	21	27	146
I/O	24	B9	22	28	149
I/O	-	A9	23	29	152
I/O	-	B10	24	30	155
-	-	-	-	31*	-
-	-	-	-	32*	-
I/O	25	C10	25	33	158
I/O	26	A10	26	34	161
I/O	-	A11	27	35	164
I/O	-	B11	28	36	167
GND	-	C11	29	37	-
-	-	-	-	38*	-
-	-	-	-	39*	-
I/O	-	A12	30	40	170
I/O	-	-	31	41	173
I/O	27	B12	32	42	176
I/O	-	A13	33	43	179
I/O	-	A14	34	44	182
I/O	-	C12	35	45	185
I/O	28	B13	36	46	188
SGCK2 (I/O)	29	B14	37	47	191
O (M1)	30	A15	38	48	194
GND	31	C13	39	49	-
I (M0)	32	A16	40	50	197†
-	-	-	-	51*	-
-	-	-	-	52*	-
-	-	-	-	53*	-
-	-	-	-	54*	-
VCC	33	C14	41	55	-
I (M2)	34	B15	42	56	198†
PGCK2 (I/O)	35	B16	43	57	199
I/O (HDC)	36	D14	44	58	202
I/O	-	C15	45	59	205
I/O	-	D15	46	60	208
I/O	-	E14	47	61	211
I/O ($\overline{\text{LDC}}$)	37	C16	48	62	214
I/O	-	E15	49	63	217
I/O	-	D16	50	64	220
-	-	-	-	65*	-
-	-	-	-	66*	-
GND	-	F14	51	67	-
I/O	-	F15	52	68	223
I/O	-	E16	53	69	226
I/O	38	F16	54	70	229
I/O	39	G14	55	71	232
-	-	-	-	72*	-
-	-	-	-	73*	-
I/O	-	G15	56	74	235
I/O	-	G16	57	75	238
I/O	40	H16	58	76	241
I/O ($\overline{\text{ERR}}$,$\overline{\text{INIT}}$)	41	H15	59	77	244
VCC	42	H14	60	78	-

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4006 Pinouts (continued)

Pin Description	PC 84	PG 156	PQ1 60	PQ 208	Boundary Scan Order
GND	43	J14	61	79	-
I/O	44	J15	62	80	247
I/O	45	J16	63	81	250
I/O	-	K16	64	82	253
I/O	-	K15	65	83	256
-	-	-	-	84*	-
-	-	-	-	85*	-
I/O	46	K14	66	86	259
I/O	47	L16	67	87	262
I/O	-	M16	68	88	265
I/O	-	L15	69	89	268
GND	-	L14	70	90	-
-	-	-	-	91*	-
-	-	-	-	92*	-
I/O	-	N16	71	93	271
I/O	-	M15	72	94	274
I/O	48	P16	73	95	277
I/O	49	M14	74	96	280
I/O	-	N15	75	97	283
I/O	-	P15	76	98	286
I/O	50	N14	77	99	289
SGCK3 (I/O)	51	R16	78	100	292
GND	52	P14	79	101	-
-	-	-	-	102*	-
DONE	53	R15	80	103	-
-	-	-	-	104*	-
-	-	-	-	105*	-
VCC	54	P13	81	106	-
-	-	-	-	107*	-
$\overline{PROG}$	55	R14	82	108	-
I/O (D7)	56	T16	83	109	295
PGCK3 (I/O)	57	T15	84	110	298
I/O	-	R13	85	111	301
I/O	-	P12	86	112	304
I/O (D6)	58	T14	87	113	307
I/O	-	T13	88	114	310
I/O	-	R12	89	115	313
I/O	-	T12	90	116	316
-	-	-	-	117*	-
-	-	-	-	118*	-
GND	-	P11	91	119	-
I/O	-	R11	92	120	319
I/O	-	T11	93	121	322
I/O (D5)	59	T10	94	122	325
I/O ($\overline{CS0}$)	60	P10	95	123	328
-	-	-	-	124*	-
-	-	-	-	125*	-
I/O	-	R10	96	126	331
I/O	-	T9	97	127	334
I/O (D4)	61	R9	98	128	337
I/O	62	P9	99	129	340
VCC	63	R8	100	130	-

* Indicates unconnected package pins.

Pin Description	PC 84	PG 156	PQ 160	PQ 208	Boundary Scan Order
GND	64	P8	101	131	-
I/O (D3)	65	T8	102	132	343
I/O ($\overline{RS}$)	66	T7	103	133	346
I/O	-	T6	104	134	349
I/O	-	R7	105	135	352
-	-	-	-	136*	-
-	-	-	-	137*	-
I/O (D2)	67	P7	106	138	355
I/O	68	T5	107	139	358
I/O	-	R6	108	140	361
I/O	-	T4	109	141	364
GND	-	P6	110	142	-
-	-	-	-	143*	-
-	-	-	-	144*	-
I/O	-	R5	111	145	367
I/O	-	-	112	146	370
I/O (D1)	69	T3	113	147	373
I/O (RCLK-BUSY/$\overline{RDY}$)	70	P5	114	148	376
I/O	-	R4	115	149	379
I/O	-	R3	116	150	382
I/O (D0, DIN)	71	P4	117	151	385
SGCK4 (DOUT, I/O)	72	T2	118	152	388
CCLK	73	R2	119	153	-
VCC	74	P3	120	154	-
-	-	-	-	155*	-
-	-	-	-	156*	-
-	-	-	-	157*	-
-	-	-	-	158*	-
TDO	75	T1	121	159	-
GND	76	N3	122	160	-
I/O (A0, $\overline{WS}$)	77	R1	123	161	2
PGCK4 (I/O, A1)	78	P2	124	162	5
I/O	-	N2	125	163	8
I/O	-	M3	126	164	11
I/O (CS1,A2)	79	P1	127	165	14
I/O (A3)	80	N1	128	166	17
I/O	-	M2	129	167	20
I/O	-	M1	130	168	23
-	-	-	-	169*	-
-	-	-	-	170*	-
GND	-	L3	131	171	-
I/O	-	L2	132	172	26
I/O	-	L1	133	173	29
I/O (A4)	81	K3	134	174	32
I/O (A5)	82	K2	135	175	35
-	-	-	-	176*	-
-	-	-	136*	177*	-
I/O	-	K1	137	178	38
I/O	-	J1	138	179	41
I/O (A6)	83	J2	139	180	44
I/O (A7)	84	J3	140	181	47
GND	1	H2	141	182	-

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 391 = BSCAN.UPD

XC4008 Pinouts

Pin Description	PC 84	PQ 160	PG 191	PQ 208	Boundary Scan Order
VCC	2	142	J4	183	–
I/O (A8)	3	143	J3	184	56
I/O (A9)	4	144	J2	185	59
I/O	–	145	J1	186	62
I/O	–	146	H1	187	65
I/O	–	–	H2	188	68
I/O	–	–	H3	189	71
I/O (A10)	5	147	G1	190	74
I/O (A11)	6	148	G2	191	77
I/O	–	149	F1	192	80
I/O	–	150	E1	193	83
GND	–	151	G3	194	–
–	–	–	F2*	195*	–
–	–	–	D1*	196*	–
I/O	–	152	C1	197	86
I/O	–	153	E2	198	89
I/O (A12)	7	154	F3	199	92
I/O (A13)	8	155	D2	200	95
I/O	–	156	B1	201	98
–	–	–	–	–	–
I/O	–	157	E3	202	101
I/O (A14)	9	158	C2	203	104
SGCK1 (A15, I/O)	10	159	B2	204	107
VCC	11	160	D3	205	–
–	–	–	–	206*	–
–	–	–	–	207*	–
–	–	–	–	208*	–
–	–	–	–	1*	–
GND	12	1	D4	2	–
–	–	–	–	3*	–
PGCK1 (A16, I/O)	13	2	C3	4	110
I/O (A17)	14	3	C4	5	113
I/O	–	4	B3	6	116
–	–	–	–	–	–
I/O	–	5	C5	7	119
I/O (TDI)	15	6	A2	8	122
I/O (TCK)	16	7	B4	9	125
I/O	–	8	C6	10	128
I/O	–	9	A3	11	131
–	–	–	B5*	12*	–
–	–	–	B6*	13*	–
GND	–	10	C7	14	–
I/O	–	11	A4	15	134
I/O	–	12	A5	16	137
I/O (TMS)	17	13	B7	17	140
I/O	18	14	A6	18	143
I/O	–	–	C8	19	146
I/O	–	–	A7	20	149
I/O	–	15	B8	21	152
I/O	–	16	A8	22	155
I/O	19	17	B9	23	158
I/O	20	18	C9	24	161
GND	21	19	D9	25	–

Pin Description	PC 84	PQ 160	PG 191	PQ 208	Boundary Scan Order
VCC	22	20	D10	26	–
I/O	23	21	C10	27	164
I/O	24	22	B10	28	167
I/O	–	23	A9	29	170
I/O	–	24	A10	30	173
I/O	–	–	A11	31	176
I/O	–	–	C11	32	179
I/O	25	25	B11	33	182
I/O	26	26	A12	34	185
I/O	–	27	B12	35	188
I/O	–	28	A13	36	191
GND	–	29	C12	37	–
–	–	–	B13*	38*	–
–	–	–	A14*	39*	–
I/O	–	30	A15	40	194
I/O	–	31	C13	41	197
I/O	27	32	B14	42	200
I/O	–	33	A16	43	203
I/O	–	34	B15	44	206
I/O	–	35	C14	45	209
I/O	28	36	A17	46	212
SGCK2 (I/O)	29	37	B16	47	215
O (M1)	30	38	C15	48	218
GND	31	39	D15	49	–
I (M0)	32	40	A18	50	221†
–	–	–	–	51*	–
–	–	–	–	52*	–
–	–	–	–	53*	–
–	–	–	–	54*	–
VCC	33	41	D16	55	–
I (M2)	34	42	C16	56	222†
PGCK2 (I/O)	35	43	B17	57	223
I/O (HDC)	36	44	E16	58	226
–	–	–	–	–	–
I/O	–	45	C17	59	229
I/O	–	46	D17	60	232
I/O	–	47	B18	61	235
I/O (LDC)	37	48	E17	62	238
I/O	–	49	F16	63	241
I/O	–	50	C18	64	244
–	–	–	D18*	65*	–
–	–	–	F17*	66*	–
GND	–	51	G16	67	–
I/O	–	52	E18	68	247
I/O	–	53	F18	69	250
I/O	38	54	G17	70	253
I/O	39	55	G18	71	256
I/O	–	–	H16	72	259
I/O	–	–	H17	73	262
I/O	–	56	H18	74	265
I/O	–	57	J18	75	268
I/O	40	58	J17	76	271
I/O (ERR, INIT)	41	59	J16	77	274
VCC	42	60	J15	78	–

* Indicates unconnected package pins.

† Contributes only one bit (.i) to the boundary scan register.

XC4008 Pinouts (continued)

Pin Description	PC 84	PQ 160	PG 191	PQ 208	Boundary Scan Order
GND	43	61	K15	79	–
I/O	44	62	K16	80	277
I/O	45	63	K17	81	280
I/O	–	64	K18	82	283
I/O	–	65	L18	83	286
I/O	–	–	L17	84	289
I/O	–	–	L16	85	292
I/O	46	66	M18	86	295
I/O	47	67	M17	87	298
I/O	–	68	N18	88	301
I/O	–	69	P18	89	304
GND	–	70	M16	90	–
–	–	–	N17*	91*	–
–	–	–	R18*	92*	–
I/O	–	71	T18	93	307
I/O	–	72	P17	94	310
I/O	48	73	N16	95	313
I/O	49	74	T17	96	316
I/O	–	75	R17	97	319
I/O	–	76	P16	98	322
I/O	50	77	U18	99	325
SGCK3 (I/O)	51	78	T16	100	328
GND	52	79	R16	101	–
–	–	–	–	102*	–
DONE	53	80	U17	103	–
–	–	–	–	104*	–
–	–	–	–	105*	–
VCC	54	81	R15	106	–
–	–	–	–	107*	–
$\overline{PROG}$	55	82	V18	108	–
I/O (D7)	56	83	T15	109	331
PGCK3 (I/O)	57	84	U16	110	334
–	–	–	–	–	–
I/O	–	85	T14	111	337
I/O	–	86	U15	112	340
I/O (D6)	58	87	V17	113	343
I/O	–	88	V16	114	346
I/O	–	89	T13	115	349
I/O	–	90	U14	116	352
–	–	–	V15*	117*	–
–	–	–	V14*	118*	–
GND	–	91	T12	119	–
I/O	–	92	U13	120	355
I/O	–	93	V13	121	358
I/O (D5)	59	94	U12	122	361
I/O ($\overline{CSO}$)	60	95	V12	123	364
I/O	–	–	T11	124	367
I/O	–	–	U11	125	370
I/O	–	96	V11	126	373
I/O	–	97	V10	127	376
I/O (D4)	61	98	U10	128	379
I/O	62	99	T10	129	382
VCC	63	100	R10	130	
GND	64	101	R9	131	

Pin Description	PC 84	PQ 160	PG 191	PQ 208	Boundary Scan Order
I/O (D3)	65	102	T9	132	385
I/O ($\overline{RS}$)	66	103	U9	133	388
I/O	–	104	V9	134	391
I/O	–	105	V8	135	394
I/O	–	–	U8	136	397
I/O	–	–	T8	137	400
I/O (D2)	67	106	V7	138	403
I/O	68	107	U7	139	406
I/O	–	108	V6	140	409
I/O	–	109	U6	141	412
GND	–	110	T7	142	–
–	–	–	V5*	143*	–
–	–	–	V4*	144*	–
I/O	–	111	U5	145	415
I/O	–	112	T6	146	418
I/O (D1)	69	113	V3	147	421
I/O ($\overline{RCLK}$-$\overline{BUSY}$/RDY)	70	114	V2	148	424
I/O	–	115	U4	149	427
I/O	–	116	T5	150	430
I/O (D0, DIN)	71	117	U3	151	433
SGCK4 (DOUT, I/O)	72	118	T4	152	436
CCLK	73	119	V1	153	–
VCC	74	120	R4	154	–
–	–	–	–	155*	–
–	–	–	–	156*	–
–	–	–	–	157*	–
–	–	–	–	158*	–
TDO	75	121	U2	159	–
GND	76	122	R3	160	–
I/O (A0, $\overline{WS}$)	77	123	T3	161	2
PGCK4 (I/O,A1)	78	124	U1	162	5
–	–	–	–	–	–
I/O	–	125	P3	163	8
I/O	–	126	R2	164	11
I/O (CS1, A2)	79	127	T2	165	14
I/O (A3)	80	128	N3	166	17
I/O	–	129	P2	167	20
I/O	–	130	T1	168	23
–	–	–	R1*	169*	–
–	–	–	N2*	170*	–
GND	–	131	M3	171	–
I/O	–	132	P1	172	26
I/O	–	133	N1	173	29
I/O (A4)	81	134	M2	174	32
I/O (A5)	82	135	M1	175	35
I/O	–	–	L3	176	38
I/O	–	136	L2	177	41
I/O	–	137	L1	178	44
I/O	–	138	K1	179	47
I/O (A6)	83	139	K2	180	50
I/O (A7)	84	140	K3	181	53
GND	1	141	K4	182	–

* Indicates unconnected package pins.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 439 = BSCAN.UPD

XC4010/XC4010D Pinouts

Pin Description	PC84	PQ160	†† PG191	PQ208	*** BG225	Boundary Scan Order
VCC	2	142	J4	183	D8	-
I/O (A8)	3	143	J3	184	E8	62
I/O (A9)	4	144	J2	185	B7	65
I/O	-	145	J1	186	A7	68
I/O	-	146	H1	187	C7	71
I/O	-	-	H2	188	D7	74
I/O	-	-	H3	189	E7	77
I/O (A10)	5	147	G1	190	A6	80
I/O (A11)	6	148	G2	191	B6	83
I/O	-	149	F1	192	A5	86
I/O	-	150	E1	193	B5	89
GND	-	151	G3	194	**	-
I/O	-	-	F2	195	D6	92
I/O	-	-	D1	196	C5	96
I/O	-	152	C1	197	A4	98
I/O	-	153	E2	198	E6	101
I/O (A12)	7	154	F3	199	B4	104
I/O (A13)	8	155	D2	200	D5	107
I/O	-	156	B1	201	B3	110
I/O	-	157	E3	202	F6	113
I/O (A14)	9	158	C2	203	A2	116
SGCK1 (A15, I/O)	10	159	B2	204	C3	119
VCC	11	160	D3	205	B2	-
-	-	-	-	206*	-	-
-	-	-	-	207*	-	-
-	-	-	-	208*	-	-
-	-	-	-	1*	-	-
GND	12	1	D4	2	A1	-
-	-	-	-	3*	-	-
PGCK1 (A16, I/O)	13	2	C3	4	D4	122
I/O (A17)	14	3	C4	5	B1	125
I/O	-	4	B3	6	C2	128
I/O	-	5	C5	7	E5	131
I/O (TDI)	15	6	A2	8	D3	134
I/O (TCK)	16	7	B4	9	C1	137
I/O	-	8	C6	10	D2	140
I/O	-	9	A3	11	G6	143
I/O	-	-	B5	12	E4	146
I/O	-	-	B6	13	D1	149
GND	-	10	C7	14	**	-
I/O	-	11	A4	15	F5	152
I/O	-	12	A5	16	E1	155
I/O (TMS)	17	13	B7	17	F4	158
I/O	18	14	A6	18	F3	161
I/O	-	-	C8	19	G4	164
I/O	-	-	A7	20	G3	167
I/O	-	15	B8	21	G2	170
I/O	-	16	A8	22	G1	173
I/O	19	17	B9	23	G5	176
I/O	20	18	C9	24	H3	179
GND	21	19	D9	25	H2	-
VCC	22	20	D10	26	H1	-
I/O	23	21	C10	27	H4	182
I/O	24	22	B10	28	H5	185
I/O	-	23	A9	29	J2	188

Pin Description	PC84	PQ160	PG191	PQ208	*** BG225	Boundary Scan Order
I/O	-	24	A10	30	J1	191
I/O	-	-	A11	31	J3	194
I/O	-	-	C11	32	J4	197
I/O	25	25	B11	33	K2	200
I/O	26	26	A12	34	K3	203
I/O	-	27	B12	35	J6	206
I/O	-	28	A13	36	L1	209
GND	-	29	C12	37	**	-
I/O	-	-	B13	38	L3	212
I/O	-	-	A14	39	M1	215
I/O	-	30	A15	40	K5	218
I/O	-	31	C13	41	M2	221
I/O	27	32	B14	42	L4	224
I/O	-	33	A16	43	N1	227
I/O	-	34	B15	44	M3	230
I/O	-	35	C14	45	N2	233
I/O	28	36	A17	46	K6	236
SGCK2 (I/O)	29	37	B16	47	P1	239
O (M1)	30	38	C15	48	N3	242
GND	31	39	D15	49	**	-
I (M0)	32	40	A18	50	P2	245†
-	-	-	-	51*	-	-
-	-	-	-	52*	-	-
-	-	-	-	53*	-	-
-	-	-	-	54*	-	-
VCC	33	41	D16	55	R1	-
I (M2)	34	42	C16	56	M4	246†
PGCK2 (I/O)	35	43	B17	57	R2	247
I/O (HDC)	36	44	E16	58	P3	250
I/O	-	45	C17	59	L5	253
I/O	-	46	D17	60	N4	256
I/O	-	47	B18	61	R3	259
I/O (LDC)	37	48	E17	62	P4	262
I/O	-	49	F16	63	K7	265
I/O	-	50	C18	64	M5	268
I/O	-	-	D18	65	R4	271
I/O	-	-	F17	66	N5	274
GND	-	51	G16	67	**	-
I/O	-	52	E18	68	R5	277
I/O	-	53	F18	69	M6	280
I/O	38	54	G17	70	N6	283
I/O	39	55	G18	71	P6	286
I/O	-	-	H16	72	R6	289
I/O	-	-	H17	73	M7	291
I/O	-	56	H18	74	R7	295
I/O	-	57	J18	75	L7	298
I/O	40	58	J17	76	N8	301
I/O ($\overline{ERR}$, $\overline{INIT}$)	41	59	J16	77	P8	304
VCC	42	60	J15	78	R8	-
GND	43	61	K15	79	M8	-
I/O	44	62	K16	80	L8	307
I/O	45	63	K17	81	P9	310
I/O	-	64	K18	82	R9	313
I/O	-	65	L18	83	N9	316
I/O	-	-	L17	84	M9	319
I/O	-	-	L16	85	L9	322
I/O	46	66	M18	86	N10	325

* Indicates unconnected package pins.

** The following BGA225 balls are connected to ground: F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8

*** The following BG225 balls are unconnected: E3, E2, F1, F2, J5, K1, L2, K4, P5, L6, N7, P7, R10, P10, M10, N11, N15, M14, L15, K12, G10, E15, E14, F12, F9, D11, C10, B10, C6, F7, A3, C4

† Contributes only one bit (.i) to the boundary scan register.

†† XC4010 only. PG191 package not available for XC4010D

XC4010/XC4010D Pinouts (continued)

Pin Description	PC84	†† PQ160	PG191	PQ208	*** BG225	Boundary Scan Order
I/O	47	67	M17	87	K9	328
I/O	-	68	N18	88	R11	331
I/O	-	69	P18	89	P11	334
GND	-	70	M16	90	**	-
I/O	-	-	N17	91	R12	337
I/O	-	-	R18	92	L10	340
I/O	-	71	T18	93	P12	343
I/O	-	72	P17	94	M11	346
I/O	48	73	N16	95	R13	349
I/O	49	74	T17	96	N12	352
I/O	-	75	R17	97	P13	355
I/O	-	76	P16	98	K10	358
I/O	50	77	U18	99	R14	361
SGCK3 (I/O)	51	78	T16	100	N13	364
GND	52	79	R16	101	**	-
-	-	-	-	102*	-	-
DONE	53	80	U17	103	P14	-
-	-	-	-	104*	-	-
-	-	-	-	105*	-	-
VCC	54	81	R15	106	R15	-
-	-	-	-	107*	-	-
$\overline{PROG}$	55	82	V18	108	M12	-
I/O (D7)	56	83	T15	109	P15	367
PGCK3 (I/O)	57	84	U16	110	N14	370
I/O	-	85	T14	111	L11	373
I/O	-	86	U15	112	M13	376
I/O (D6)	58	87	V17	113	J10	379
I/O	-	88	V16	114	L12	382
I/O	-	89	T13	115	M15	385
I/O	-	90	U14	116	L13	388
I/O	-	-	V15	117	L14	391
I/O	-	-	V14	118	K11	394
GND	-	91	T12	119	**	-
I/O	-	92	U13	120	K13	397
I/O	-	93	V13	121	K14	400
I/O (D5)	59	94	U12	122	K15	403
I/O ($\overline{CSO}$)	60	95	V12	123	J12	406
I/O	-	-	T11	124	J13	409
I/O	-	-	U11	125	J14	412
I/O	-	96	V11	126	J15	415
I/O	-	97	V10	127	J11	418
I/O (D4)	61	98	U10	128	H13	421
I/O	62	99	T10	129	H14	424
VCC	63	100	R10	130	H15	-
GND	64	101	R9	131	**	-
I/O (D3)	65	102	T9	132	H12	427
I/O ($\overline{RS}$)	66	103	U9	133	H11	430
I/O	-	104	V9	134	G14	433
I/O	-	105	V8	135	G15	436
I/O	-	-	U8	136	G13	439
I/O	-	-	T8	137	G12	442
I/O (D2)	67	106	V7	138	G11	445
I/O	68	107	U7	139	F15	448
I/O	-	108	V6	140	F14	451
I/O	-	109	U6	141	F13	454
GND	-	110	T7	142	**	-
I/O	-	-	V5	143	E13	457

Pin Description	PC84	PQ160	PG191	PQ208	*** BG225	Boundary Scan Order
I/O	-	-	V4	144	D15	460
I/O	-	111	U5	145	F11	463
I/O	-	112	T6	146	D14	466
I/O (D1)	69	113	V3	147	E12	469
I/O ($\overline{RCLK}$-$\overline{BUSY}$/RDY	70	114	V2	148	C15	472
I/O	-	115	U4	149	D13	475
I/O	-	116	T5	150	C14	478
I/O (D0, DIN)	71	117	U3	151	F10	481
SGCK4 (DOUT, I/O)	72	118	T4	152	B15	484
CCLK	73	119	V1	153	C13	-
VCC	74	120	R4	154	B14	-
-	-	-	-	155*	-	-
-	-	-	-	156*	-	-
-	-	-	-	157*	-	-
-	-	-	-	158*	-	-
TDO	75	121	U2	159	A15	-
GND	76	122	R3	160	D12	-
I/O (A0, $\overline{WS}$)	77	123	T3	161	A14	2
PGCK4 (I/O, A1)	78	124	U1	162	B13	5
I/O	-	125	P3	163	E11	8
I/O	-	126	R2	164	C12	11
I/O (CS1, A2)	79	127	T2	165	A13	14
I/O (A3)	80	128	N3	166	B12	17
I/O	-	129	P2	167	A12	20
I/O	-	130	T1	168	C11	23
I/O	-	-	R1	169	B11	26
I/O	-	-	N2	170	E10	29
GND	-	131	M3	171	**	-
I/O	-	132	P1	172	A11	32
I/O	-	133	N1	173	D10	35
I/O (A4)	81	134	M2	174	A10	38
I/O (A5)	82	135	M1	175	D9	41
I/O	-	-	L3	176	C9	44
I/O	-	136	L2	177	B9	47
I/O	-	137	L1	178	A9	50
I/O	-	138	K1	179	B8	53
I/O (A6)	83	139	K2	180	C8	56
I/O (A7)	84	140	K3	181	B8	59
GND	1	141	K4	182	A8	-

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 487 = BSCAN.UPD

* Indicates unconnected package pins.

** The following BGA225 balls are connected to ground:
F8, G7, G8, G9, H6, H7, H8, H9, H10, J7, J8, J9, K8

*** The following BG225 balls are unconnected:
E3, E2, F1, F2, J5, K1, L2, K4, P5, L6, N7, P7, R10, P10, M10, N11, N15, M14, L15, K12, G10, E15, E14, F12, F9, D11, C10, B10, C6, F7, A3, C4

†† XC4010 only. PG 191 package not available for XC4010D

XC4013/XC4013D Pinouts

Pin Description	PQ160	MQ208	PG223	BG225	PQ240	Boundary Scan Order
VCC	142	183	J4	A10	212	-
I/O (A8)	143	184	J3	E8	213	74
I/O (A9)	144	185	J2	F8	214	77
I/O	145	186	J1	B7	215	80
I/O	146	187	H1	A7	216	83
I/O	-	188	H2	G7	217	86
I/O	-	189	H3	E7	218	89
-	-	-	-	-	219*	-
I/O (A10)	147	190	G1	F7	220	92
I/O (A11)	148	191	G2	C7	221	95
VCC	-	-	-	-	222	-
I/O	-	-	H4	B6	223	98
I/O	-	-	G4	E6	224	101
I/O	149	192	F1	D7	225	104
I/O	150	193	E1	F6	226	107
GND	151	194	G3	A5	227	-
I/O	-	195	F2	B5	228	110
I/O	-	196	D1	D5	229	113
I/O	152	197	C1	C5	230	116
I/O	153	198	E2	C6	231	119
I/O (A12)	154	199	F3	A4	232	122
I/O (A13)	155	200	D2	D4	233	125
I/O	-	-	F4	B4	234	128
I/O	-	-	E4	C3	235	131
I/O	156	201	B1	A3	236	134
I/O	157	202	E3	C2	237	137
I/O (A14)	158	203	C2	D6	238	140
SGCK1 (A15, I/O)	159	204	B2	A2	239	143
VCC	160	205	D3	A6	240	-
-	-	206*	-	-	-	-
-	-	207*	-	-	-	-
-	-	208*	-	-	-	-
-	-	1*	-	-	-	-
GND	1	2	D4	A1	1	-
-	-	3*	-	-	-	-
PGCK1 (A16,I/O)	2	4	C3	B1	2	146
I/O (A17)	3	5	C4	B3	3	149
I/O	4	6	B3	C4	4	152
I/O	5	7	C5	B2	5	155
I/O (TDI)	6	8	A2	C1	6	158
I/O (TCK)	7	9	B4	E3	7	161
I/O	8	10	C6	D2	8	164
I/O	9	11	A3	D3	9	167
I/O	-	12	B5	D1	10	170
I/O	-	13	B6	E5	11	173
I/O	-	-	D5	F4	12	176
I/O	-	-	D6	E2	13	179
GND	10	14	C7	E1	14	-
I/O	11	15	A4	E4	15	182
I/O	12	16	A5	F3	16	185
I/O (TMS)	13	17	B7	F2	17	188
I/O	14	18	A6	F5	18	191
VCC	-	-	-	F1	19	-
I/O	-	-	D7	G4	20	194
I/O	-	-	D8	G2	21	197
-	-	-	-	-	22*	-
I/O	-	19	C8	G3	23	200
I/O	-	20	A7	G6	24	203
I/O	15	21	B8	G5	25	206
I/O	16	22	A8	G1	26	209
I/O	17	23	B9	H5	27	212
I/O	18	24	C9	H7	28	215
GND	19	25	D9	H1	29	-
VCC	20	26	D10	H2	30	-

Pin Description	PQ160	MQ208	PG223	BG225	PQ240	Boundary Scan Order
I/O	21	27	C10	H6	31	218
I/O	22	28	B10	H3	32	221
I/O	23	29	A9	J6	33	224
I/O	24	30	A10	H4	34	227
I/O	-	31	A11	J1	35	230
I/O	-	32	C11	J5	36	233
-	-	-	-	-	37*	-
I/O	-	-	D11	J2	38	236
I/O	-	-	D12	J7	39	239
VCC	-	-	-	K1	40	-
I/O	25	33	B11	J3	41	242
I/O	26	34	A12	K2	42	245
I/O	27	35	B12	K5	43	248
I/O	28	36	A13	K3	44	251
GND	29	37	C12	L1	45	-
I/O	-	-	D13	K6	46	254
I/O	-	-	D14	L2	47	257
I/O	-	38	B13	J4	48	260
I/O	-	39	A14	M2	49	263
I/O	30	40	A15	L5	50	266
I/O	31	41	C13	M1	51	269
I/O	32	42	B14	H3	52	272
I/O	33	43	A16	L3	53	275
I/O	34	44	B15	M4	54	278
I/O	35	45	C14	N1	55	281
I/O	36	46	A17	N2	56	284
SGCK2 (I/O)	37	47	B16	K4	57	287
O (M1)	38	48	C15	L4	58	290
GND	39	49	D15	41	59	-
I (M0)	40	50	A18	P1	60	293†
-	-	51*	-	-	-	-
-	-	52*	-	-	-	-
-	-	53*	-	-	-	-
-	-	54*	-	-	-	-
VCC	41	55	D16	R6	61	-
I (M2)	42	56	C16	R2	62	294†
PGCK2 (I/O)	43	57	B17	P3	63	295
I/O (HDC)	44	58	E16	M6	64	298
I/O	45	59	C17	P2	65	301
I/O	46	60	D17	R3	66	304
I/O	47	61	B18	N3	67	307
I/O (LDC)	48	62	E17	N5	68	310
I/O	49	63	F16	N4	69	313
I/O	50	64	C18	R4	70	316
I/O	-	65	D18	P4	71	319
I/O	-	66	F17	N6	72	322
I/O	-	-	E15	P5	73	325
I/O	-	-	F15	M5	74	328
GND	51	67	G16	R5	75	-
I/O	52	68	E18	M7	76	331
I/O	53	69	F18	P6	77	334
I/O	54	70	G17	L6	78	337
I/O	55	71	G18	N7	79	340
VCC	-	-	-	-	80	-
I/O	-	72	H16	P7	81	343
I/O	-	73	H17	M8	82	346
-	-	-	-	-	83*	-
I/O	-	-	G15	K7	84	349
I/O	-	-	H15	L7	85	352
I/O	56	74	H18	R7	86	355
I/O	57	75	J18	N8	87	358
I/O	58	76	J17	J8	88	361
I/O (ERR, INIT)	59	77	J16	P8	89	364
VCC	60	78	J15	R10	90	-

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.

XC4013/XC4013D Pinouts (continued)

Pin Description	PQ160	MQ208	PQ223	BG225	PQ240	Boundary Scan Order
GND	61	79	K15	R8	91	-
I/O	62	80	K16	L8	92	367
I/O	63	81	K17	M9	93	370
I/O	64	82	K18	P9	94	373
I/O	65	83	L18	R9	95	376
I/O	-	84	L17	K8	96	379
I/O	-	85	L16	L9	97	382
-	-	-	-	-	98*	-
I/O	-	-	L15	K9	99	385
I/O	-	-	M15	N9	100	388
VCC	-	-	-	-	101	-
I/O	66	86	M18	P10	102	391
I/O	67	87	M17	L10	103	394
I/O	68	88	N18	N10	104	397
I/O	69	89	P18	K10	105	400
GND	70	90	M16	R11	106	-
I/O	-	-	N15	N11	107	403
I/O	-	-	P15	P11	108	406
I/O	-	91	N17	M10	109	409
I/O	-	92	R18	P12	110	412
I/O	71	93	T18	R12	111	415
I/O	72	94	P17	N12	112	418
I/O	73	95	N16	K12	113	421
I/O	74	96	T17	P13	114	424
I/O	75	97	R17	R13	115	427
I/O	76	98	P16	P14	116	430
I/O	77	99	U18	K13	117	433
SGCK3 (I/O)	78	100	T16	M13	118	0
GND	79	101	R16	R15	119	-
-	-	102*	-	-	-	-
DONE	80	103	U17	R14	120	-
-	-	104*	-	-	-	-
-	-	105*	-	-	-	-
VCC	81	106	R15	K15	121	-
-	-	107*	-	-	-	-
$\overline{PROG}$	82	108	V18	P15	122	-
I/O (D7)	83	109	T15	N14	123	439
PGCK3 (I/O)	84	110	U16	L13	124	442
I/O	85	111	T14	N13	125	445
I/O	86	112	U15	N15	126	448
I/O	-	-	R14	M11	127	451
I/O	-	-	R13	M14	128	454
I/O (D6)	87	113	V17	M12	129	457
I/O	88	114	V16	M15	130	460
I/O	89	115	T13	L11	131	463
I/O	90	116	U14	J12	132	466
I/O	-	117	V15	L14	133	469
I/O	-	118	V14	L12	134	472
GND	91	119	T12	L15	135	-
I/O	-	-	R12	J13	136	475
I/O	-	-	R11	K14	137	478
I/O	92	120	U13	K11	138	481
I/O	93	121	V13	H11	139	484
VCC	-	-	-	-	140	-
I/O (D5)	94	122	U12	J14	141	487
I/O ($\overline{CSO}$)	95	123	V12	H12	142	490
-	-	-	-	-	143*	-
I/O	-	124	T11	J10	144	493
I/O	-	125	U11	J11	145	496
I/O	96	126	V11	J15	146	499
I/O	97	127	V10	H13	147	502
I/O (D4)	98	128	U10	J9	148	505
I/O	99	129	T10	H9	149	508
VCC	100	130	R10	H14	150	-

Pin Description	PQ160	MQ208	PQ223	BG225	PQ240	Boundary Scan Order
GND	101	131	R9	H15	151	-
I/O (D3)	102	132	T9	H10	152	511
I/O ($\overline{RS}$)	103	133	U9	G12	153	514
I/O	104	134	V9	G14	154	517
I/O	105	135	V8	G15	155	520
I/O	-	136	U8	G9	156	523
I/O	-	137	T8	G11	157	526
-	-	-	-	-	158*	-
I/O (D2)	106	138	V7	G10	159	529
I/O	107	139	U7	G13	160	532
VCC	-	-	-	-	161	-
I/O	108	140	V6	F14	162	535
I/O	109	141	U6	F11	163	538
I/O	-	-	R8	F13	164	541
I/O	-	-	R7	F10	165	544
GND	110	142	T7	E15	166	-
I/O	-	-	R6	E14	167	547
I/O	-	-	R5	F12	168	550
I/O	-	143	V5	D14	169	553
I/O	-	144	V4	E12	170	556
I/O	111	145	U5	D15	171	559
I/O	112	146	T6	D13	172	562
I/O (D1)	113	147	V3	E13	173	565
I/O (RCLK-$\overline{BUSY}$/RDY)	114	148	V2	C13	174	568
I/O	115	149	U4	C15	175	571
I/O	116	150	T5	C14	176	574
I/O (D0, DIN)	117	151	U3	D10	177	577
SGCK4 (DOUT, I/O)	118	152	T4	C11	178	580
CCLK	119	153	V1	B15	179	-
VCC	120	154	R4	F15	180	-
-	-	155*	-	-	-	-
-	-	156*	-	-	-	-
-	-	157*	-	-	-	-
-	-	158*	-	-	-	-
TDO	121	159	U2	A14	181	-
GND	122	160	R3	A15	182	-
I/O (A0, $\overline{WS}$)	123	161	T3	C12	183	2
PGCK4 (I/O, A1)	124	162	U1	C10	184	5
I/O	125	163	P3	B14	185	8
I/O	126	164	R2	A13	186	11
I/O (CS1, A2)	127	165	T2	B13	187	14
I/O (A3)	128	166	N3	B12	188	17
I/O	-	-	P4	D12	189	20
I/O	-	-	N4	A12	190	23
I/O	129	167	P2	E11	191	26
I/O	130	168	T1	D9	192	29
I/O	-	169	R1	B11	193	32
I/O	-	170	N2	D11	194	35
-	-	-	-	-	195*	-
GND	131	171	M3	A11	196	-
I/O	132	172	P1	C9	197	38
I/O	133	173	N1	B10	198	41
I/O	-	-	M4	E10	199	44
I/O	-	-	L4	D8	200	47
VCC	-	-	-	-	201	-
I/O (A4)	134	174	M2	B9	202	50
I/O (A5)	135	175	M1	C8	203	53
-	-	-	-	-	204*	-
I/O	-	176	L3	F9	205	56
I/O	136	177	L2	E9	206	59
I/O	137	178	L1	A9	207	62
I/O	138	179	K1	B8	208	65
I/O (A6)	139	180	K2	H8	209	68
I/O (A7)	140	181	K3	G8	210	71
GND	141	182	K4	A8	211	-

* Indicates unconnected package pins.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 583 = BSCAN.UPD

XC4020 Pinouts

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
VCC	183	212	J4	K1	-
I/O (A8)	184	213	J3	K2	86
I/O (A9)	185	214	J2	K3	89
I/O	186	215	J1	K5	92
I/O	187	216	H1	K4	95
I/O	188	217	H2	J1	98
I/O	189	218	H3	J2	101
I/O (A10)	190	220	G1	H1	104
I/O (A11)	191	221	G2	J3	107
I/O	-	-	-	H2	110
I/O	-	-	-	G1	113
VCC	-	222	-	E1	-
I/O	-	223	H4	H3	116
I/O	-	224	G4	G2	119
I/O	192	225	F1	H4	122
I/O	193	226	E1	F2	125
GND	194	227	G3	F1	-
I/O	195	228	F2	D1	128
I/O	196	229	D1	G4	131
I/O	197	230	C1	E2	134
I/O	198	231	E2	F3	137
I/O (A12)	199	232	F3	G5	140
I/O (A13)	200	233	D2	C1	143
I/O	-	-	-	F4	146
I/O	-	-	-	E3	149
I/O	-	234	F4	D2	152
I/O	-	235	E4	C2	155
I/O	201	236	B1	F5	158
I/O	202	237	E3	E4	161
I/O (A14)	203	238	C2	D3	164
SGCK1(A15,I/O)	204	239	B2	C3	167
VCC	205	240	03	A2	-
GND	2	1	04	B1	-
PGCK1 (A16,I/O)	4	2	C3	D4	170
I/O (A17)	5	3	C4	B2	173
I/O	6	4	B3	B3	176
I/O	7	5	C5	E6	179
I/O (TDI)	8	6	A2	D5	182
I/O (TCK)	9	7	B4	C4	185
I/O	-	-	-	A3	188
I/O	-	-	-	D6	191
I/O	10	8	C6	E7	194
I/O	11	9	A3	B4	197
I/O	12	10	B5	C5	200
I/O	13	11	B6	A4	203
I/O	-	12	D5	D7	206
I/O	-	13	D6	C6	209
GND	14	14	C7	A5	-
I/O	15	15	A4	B6	212
I/O	16	16	A5	D8	215
I/O (TMS)	17	17	B7	C7	218
I/O	18	18	A6	B7	221
VCC	-	19	-	A6	-
I/O	-	20	D7	C8	224
I/O	-	21	D8	E9	227
I/O	-	-	-	B8	230
I/O	-	-	-	A8	233
I/O	19	23	C8	C9	236
I/O	20	24	A7	B9	239
I/O	21	25	B8	E10	242
I/O	22	26	A8	A9	245
I/O	23	27	B9	D10	248
I/O	24	28	C9	C10	251
GND	25	29	D9	A10	-
VCC	26	30	D10	A11	-
I/O	27	31	C10	B10	254
I/O	28	32	B10	B11	257
I/O	29	33	A9	C11	260
I/O	30	34	A10	E11	263
I/O	31	35	A11	D11	266
I/O	32	36	C11	A12	269
I/O	-	-	-	B12	272
I/O	-	-	-	A13	275
I/O	-	38	D11	E12	278
I/O	-	39	D12	B13	281
VCC	-	40	-	A16	-
I/O	33	41	B11	A14	284

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
I/O	34	42	A12	C13	287
I/O	35	43	B12	B14	290
I/O	36	44	A13	D13	293
GND	37	45	C12	A15	-
I/O	-	46	D13	C14	296
I/O	-	47	D14	A17	299
I/O	38	48	B13	D14	302
I/O	39	49	A14	B16	305
I/O	40	50	A15	C15	308
I/O	41	51	C13	E14	311
I/O	-	-	-	A18	314
I/O	-	-	-	D15	317
I/O	42	52	B14	C16	320
I/O	43	53	A16	B17	323
I/O	44	54	B15	B18	326
I/O	45	55	C14	E15	329
I/O	46	56	A17	D16	332
SCGK2 (I/O)	47	57	B16	C17	335
O (M1)	48	58	C15	A20	338
GND	49	59	D15	A19	-
I (M0)	50	60	A18	C18	341
VCC	55	61	D16	B20	-
I (M2)	56	62	C16	D17	342
PGCK2 (I/O)	57	63	B17	B19	343
I/O (HDC)	58	64	E16	C19	346
I/O	59	65	C17	F16	349
I/O	60	66	D17	E17	352
I/O	61	67	B18	D18	355
I/O (LDC)	62	68	E17	C20	358
I/O	-	-	-	F17	361
I/O	-	-	-	G16	364
I/O	63	69	F16	D19	367
I/O	64	70	C18	E18	370
I/O	65	71	D18	D20	373
I/O	66	72	F17	G17	376
I/O	-	73	E15	F18	379
I/O	-	74	F15	H16	382
GND	67	75	G16	E20	-
I/O	68	76	E18	H17	385
I/O	69	77	F18	G18	388
I/O	70	78	G17	G19	391
I/O	71	79	G18	H18	394
VCC	-	80	-	F20	-
I/O	72	81	H16	J16	397
I/O	73	82	H17	G20	400
I/O	-	-	-	H20	403
I/O	-	-	-	J18	406
I/O	-	84	G15	J19	409
I/O	-	85	H15	K16	412
I/O	74	86	H18	J20	415
I/O	75	87	J18	K17	418
I/O	76	88	J17	K18	421
I/O (ERR, INIT)	77	89	J16	K19	424
VCC	78	90	J15	L20	-
GND	79	91	K15	K20	-
I/O	80	92	K16	L19	427
I/O	81	93	K17	L18	430
I/O	82	94	K18	L16	433
I/O	83	95	L18	L17	436
I/O	84	96	L17	M20	439
I/O	85	97	L18	M19	442
I/O	-	-	-	N20	445
I/O	-	-	-	M18	448
I/O	-	99	L15	N19	451
I/O	-	100	M15	P20	454
VCC	-	101	-	T20	-
I/O	86	102	M18	N18	457
I/O	87	103	M17	P19	460
I/O	88	104	N18	N17	463
I/O	89	105	P18	R19	466
GND	90	106	M16	R20	-
I/O	-	107	N15	U20	469
I/O	-	108	P15	P17	472
I/O	91	109	N17	T19	475
I/O	92	110	R18	R18	478
I/O	93	111	T18	P16	481
I/O	94	112	P17	V20	484

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
I/O	-	-	-	R17	487
I/O	-	-	-	T18	490
I/O	95	113	N16	U19	493
I/O	96	114	T17	V19	496
I/O	97	115	R17	R16	499
I/O	98	116	P16	T17	502
I/O	99	117	U18	U18	505
SGCK3 (I/O)	100	118	T16	X20	508
GND	101	119	R16	W20	-
DONE	103	120	U17	V18	-
VCC	106	121	R15	X19	-
PROG	108	122	V18	U17	-
I/O (D7)	109	123	T15	W19	511
PGCK3 (I/O)	110	124	U16	W18	514
I/O	111	125	T14	T15	517
I/O	112	126	U15	U16	520
I/O	-	127	R14	V17	523
I/O	-	128	R13	X18	526
I/O	-	-	-	U15	529
I/O	-	-	-	T14	532
I/O (D6)	113	129	V17	W17	535
I/O	114	130	V16	V16	538
I/O	115	131	T13	X17	541
I/O	116	132	U14	U14	544
I/O	117	133	V15	V15	547
I/O	118	134	V14	T13	550
GND	119	135	T12	X16	-
I/O	-	136	R12	U13	553
I/O	-	137	R11	V14	556
I/O	120	138	U13	W14	559
I/O	121	139	V13	V13	562
VCC	-	140	-	X15	-
I/O (D5)	122	141	U12	T12	565
I/O (CS0)	123	142	V12	X14	568
I/O	-	-	-	X13	571
I/O	-	-	-	V12	574
I/O	124	144	T11	W12	577
I/O	125	145	U11	T11	580
I/O	126	146	V11	X12	583
I/O	127	147	V10	U11	586
I/O (D4)	128	148	U10	V11	589
I/O	129	149	T10	W11	592
VCC	130	150	R10	X10	-
GND	131	151	R9	X11	-
I/O (D3)	132	152	T9	W10	595
I/O (RS)	133	153	U9	V10	598
I/O	134	154	V9	T10	601
I/O	135	155	V8	U10	604
I/O	136	156	U8	X9	607
I/O	137	157	T8	W9	610
I/O	-	-	-	X8	613
I/O	-	-	-	V9	616
I/O (D2)	138	159	V7	W8	619
I/O	139	160	U7	X7	622
VCC	-	161	-	X5	-
I/O	140	162	V6	V8	625
I/O	141	163	U6	W7	628
I/O	-	164	R8	U8	631
I/O	-	165	R7	W6	634
GND	142	166	T7	X6	-
I/O	-	167	R6	X4	637
I/O	-	168	R5	U7	640
I/O	143	169	V5	W5	643
I/O	144	170	V4	V6	646
I/O	145	171	U5	T7	-
I/O	146	172	T6	X3	649
I/O (D1)	147	173	V3	U6	652
I/O (RCLK-BUSY/RDY)	148	174	V2	V5	655
I/O	-	-	-	W4	658
I/O	-	-	-	W3	661
I/O	149	175	U4	T6	664
I/O	150	176	T5	U5	667
I/O (D0, DIN)	151	177	U3	V4	670
SGCK4 (DOUT, I/O)	152	178	T4	X1	673
CCLK	153	179	V1	V3	-
VCC	154	180	R4	W1	-
TDO	159	181	U2	U4	-

† Contributes only one bit (.i) to the boundary scan register.

XC4020 Pinouts (continued)

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
GND	160	182	R3	X2	-
I/O (A0, WS)	161	183	T3	W2	2
PGCK4 (I/O, A1)	162	184	U1	V2	5
I/O	163	185	P3	R5	8
I/O	164	186	R2	T4	11
I/O (CS1, A2)	165	187	T2	U3	14
I/O (A3)	166	188	N3	V1	17
I/O	-	-	-	R4	20
I/O	-	-	-	P5	23
I/O	-	189	P4	U2	26
I/O	-	190	N4	T3	29

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
I/O	167	191	P2	U1	32
I/O	168	192	T1	P4	35
I/O	169	193	R1	R3	38
I/O	170	194	N2	N5	41
GND	171	196	M3	T1	-
I/O	172	197	P1	N4	44
I/O	173	198	N1	P3	47
I/O	-	199	M4	P2	50
I/O	-	200	L4	N3	53
VCC	-	201	-	R1	-
I/O	-	-	-	M5	56

Pin Description	HQ208	HQ240	PG233	PG299	Bound Scan
I/O	-	-	-	P1	59
I/O (A4)	174	202	M2	N1	62
I/O (A5)	175	203	M1	M3	65
I/O	176	205	L3	M2	68
I/O	177	206	L2	L5	71
I/O	178	207	L1	M1	74
I/O	179	208	K1	L4	77
I/O (A6)	180	209	K2	L3	80
I/O (A7)	181	210	K3	L2	83
GND	182	211	K4	L1	-

XC4025 Pinouts

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
VCC	J4	212	K1	38	-
I/O (A8)	J3	213	K2	37	98
I/O (A9)	J2	214	K3	36	101
I/O	J1	215	K5	35	104
I/O	H1	216	K4	34	107
I/O	H2	217	J1	33	110
I/O	H3	218	J2	32	113
GND	-	219	-	-	-
I/O (A10)	G1	220	H1	31	116
I/O (A11)	G2	221	J3	30	119
I/O	-	-	J4	29	122
I/O	-	-	J5	28	125
I/O	-	-	H2	27	128
I/O	-	-	G1	26	131
VCC	-	222	E1	25	-
I/O	H4	223	H3	23	134
I/O	G4	224	G2	22	137
I/O	F1	225	H4	21	140
I/O	E1	226	F2	20	143
GND	G3	227	F1	19	-
I/O	-	-	H5	18	146
I/O	-	-	G3	17	149
I/O	F2	228	D1	16	152
I/O	D1	229	G4	15	155
I/O	C1	230	E2	14	158
I/O	E2	231	F3	13	161
I/O (A12)	F3	232	G5	12	164
I/O (A13)	D2	233	C1	10	167
I/O	-	-	F4	9	170
I/O	-	-	E3	8	173
I/O	F4	234	D2	7	176
I/O	E4	235	C2	6	179
I/O	B1	236	F5	5	182
I/O	E3	237	E4	4	185
I/O (A14)	C2	238	D3	3	188
SGCK1 (A15, I/O)	B2	239	C3	2	191
VCC	D3	240	A2	1	-
GND	D4	1	B1	304	-
PGCK1 (A16, I/O)	C3	2	D4	303	194
VCC	-	-	E5	-	-
I/O (A17)	C4	3	B2	302	197
I/O	B3	4	B3	301	200
I/O	C5	5	E6	300	203
I/O (TDI)	A2	6	D5	299	206
I/O (TCK)	B4	7	C4	298	209
I/O	-	-	A3	297	212
I/O	-	-	D6	296	215
I/O	C6	8	E7	295	218
I/O	A3	9	B4	294	221
I/O	B5	10	C5	293	224
I/O	B6	11	A4	292	227
I/O	D5	12	D7	291	230
I/O	D6	13	C6	290	233
I/O	-	-	E8	289	236
I/O	-	-	B5	288	239
GND	C7	14	A5	287	-
I/O	A4	15	B6	286	242
I/O	A5	16	D8	285	245
I/O (TMS)	B7	17	C7	284	248
I/O	A6	18	B7	283	251

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
VCC	-	19	A6	-	-
I/O	D7	20	C8	280	254
I/O	D8	21	E9	279	257
GND	-	22	-	-	-
I/O	-	-	A7	278	260
I/O	-	-	D9	277	263
I/O	-	-	B8	276	266
I/O	-	-	A8	275	269
I/O	C8	23	C9	274	272
I/O	A7	24	B9	273	275
I/O	B8	25	E10	272	278
I/O	A8	26	A9	271	281
I/O	B9	27	D10	270	284
I/O	C9	28	C10	269	287
GND	D9	29	A10	268	-
VCC	D10	30	A11	267	-
I/O	C10	31	B10	266	290
I/O	B10	32	B11	265	293
I/O	A9	33	C11	264	296
I/O	A10	34	E11	263	299
I/O	A11	35	D11	262	302
I/O	C11	36	A12	261	305
I/O	-	-	B12	260	308
I/O	-	-	A13	259	311
I/O	-	-	C12	258	314
I/O	-	-	D12	257	317
I/O	-	37	-	-	-
I/O	D11	38	E12	256	320
I/O	D12	39	B13	255	323
VCC	-	40	A16	-	-
I/O	B11	41	A14	252	326
I/O	A12	42	C13	251	329
I/O	B12	43	B14	250	332
I/O	A13	44	D13	249	335
GND	C12	45	A15	248	-
I/O	-	-	B15	247	338
I/O	-	-	E13	246	341
I/O	D13	46	C14	245	344
I/O	D14	47	A17	244	347
I/O	B13	48	D14	243	350
I/O	A14	49	B16	242	353
I/O	A15	50	C15	241	356
I/O	C13	51	E14	240	359
I/O	-	-	A18	239	362
I/O	-	-	D15	238	365
I/O	B14	52	C16	237	368
I/O	A16	53	B17	236	371
I/O	B15	54	B18	235	374
I/O	C14	55	E15	234	377
I/O	A17	56	D16	233	380
SCGK2 (I/O)	B16	57	C17	232	383
O (M1)	C15	58	A20	231	386
GND	D15	59	A19	230	-
I (M0)	A18	60	C18	229	389†
VCC	D16	61	B20	228	-
I (M2)	C16	62	D17	227	390†
PGCK2 (I/O)	B17	63	B19	226	391
I/O (HDC)	E16	64	C19	225	394
GND	-	-	E16	-	-
I/O	C17	65	F16	224	397

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
I/O	D17	66	E17	223	400
I/O	B18	67	D18	222	403
I/O (LDC)	E17	68	C20	221	406
I/O	-	-	F17	220	409
I/O	-	-	G16	219	412
I/O	F16	69	D19	218	415
I/O	C18	70	E18	217	418
I/O	D18	71	D20	216	421
I/O	F17	72	G17	215	424
I/O	E15	73	F18	214	427
I/O	F15	74	H16	213	430
I/O	-	-	E19	212	433
I/O	-	-	F19	211	436
GND	G16	75	E20	210	-
I/O	E18	76	H17	209	439
I/O	F18	77	G18	208	442
I/O	G17	78	G19	207	445
I/O	G18	79	H18	206	448
VCC	-	80	F20	204	-
I/O	H16	81	J16	203	451
I/O	H17	82	G20	202	454
GND	-	83	-	-	-
I/O	J17	201	457		
I/O	H19	200	460		
I/O	H20	199	463		
I/O	J18	198	466		
I/O	G15	84	J19	197	469
I/O	H15	85	K16	196	472
I/O	H18	86	J20	195	475
I/O	J18	87	K17	194	478
I/O	J17	88	K18	193	481
I/O (ERR, INIT)	J16	89	K19	192	484
VCC	J15	90	L20	191	-
GND	K15	91	K20	190	-
I/O	K16	92	L19	189	487
I/O	K17	93	L18	188	490
I/O	K18	94	L16	188	493
I/O	L18	95	L17	187	496
I/O	L17	96	M20	185	499
I/O	L16	97	M19	184	502
I/O	-	-	N20	183	505
I/O	-	-	M18	182	508
I/O	-	-	M17	181	511
I/O	-	-	M16	180	514
GND	L15	98	-	179	-
I/O	M15	99	N19	178	517
I/O	-	100	-	-	520
I/O	-	101	T20	177	-
I/O	M18	102	N18	175	523
I/O	M17	103	P19	174	526
I/O	N18	104	N17	173	529
I/O	P18	105	R19	172	532
I/O	M16	106	R20	171	-
I/O	-	-	N16	170	535
I/O	-	-	P18	169	538
I/O	N15	107	U20	168	541
I/O	P15	108	P17	167	544
I/O	N17	109	T19	166	547
I/O	R18	110	R18	165	550
I/O	T18	111	P16	164	553

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
I/O	P17	112	V20	163	556
I/O	-	-	R17	162	559
I/O	-	-	T18	161	562
I/O	N16	113	U19	160	565
I/O	T17	114	V19	159	568
I/O	R17	115	R16	158	571
I/O	P16	116	T17	157	574
I/O	U18	117	U18	156	577
SGCK3 (I/O)	T16	118	X20	155	580
VCC	R16	-	T16	154	-
GND	-	119	W20	-	-
DONE	U17	120	V18	153	-
VCC	R15	121	X19	152	-
PROG	V18	122	U17	151	-
I/O (D7)	T15	123	W19	150	583
PGCK3 (I/O)	U16	124	W18	149	586
I/O	T14	125	T15	148	589
I/O	U15	126	U16	147	592
I/O	R14	127	V17	146	595
I/O	R13	128	X18	145	598
I/O	-	-	U15	144	601
I/O	-	-	T14	143	604
I/O (D6)	V17	129	W17	142	607
I/O	V16	130	V16	141	610
I/O	T13	131	X17	140	613
I/O	U14	132	U14	139	616
I/O	V15	133	V15	138	619
I/O	V14	134	T13	137	622
I/O	-	-	W16	136	625
I/O	-	-	W15	135	628
GND	T12	135	X16	134	-
I/O	R12	136	U13	133	631
I/O	R11	137	V14	132	634
I/O	U13	138	W14	131	637
I/O	V13	139	V13	130	640
VCC	-	140	X15	-	-
I/O (D5)	U12	141	T12	127	643
I/O (CS0)	V12	142	X14	126	646
GND	-	143	-	-	-
I/O	-	-	U12	125	649
I/O	-	-	W13	124	652
I/O	-	-	X13	123	655
I/O	-	-	V12	122	658
I/O	T11	144	W12	121	661
I/O	U11	145	T11	120	664
I/O	V11	146	X12	119	667
I/O	V10	147	U11	118	670
I/O (D4)	U10	148	V11	117	673
I/O	T10	149	W11	116	676
VCC	R10	150	X10	115	-
GND	R9	151	X11	114	-
I/O (D3)	T9	152	W10	113	679
I/O (RS)	U9	153	V10	112	682
I/O	V9	154	T10	111	685
I/O	V8	155	U10	110	688
I/O	T8	157	W9	108	694
I/O	U8	156	X9	109	691
I/O	-	-	X8	107	697
I/O	-	-	V9	106	700
I/O	-	-	U9	105	703

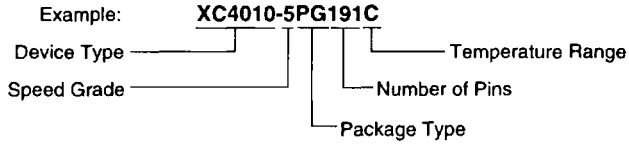
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 775 = BSCAN.UPD

XC4025 Pinouts (continued)

Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan	Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan	Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan	Pin Description	PG 223	MQ 240	PG 299	HQ 304	Bound Scan
I/O	-	-	T9	104	708	I/O	T6	172	X3	87	745	I/O	R2	186	T4	71	11	I/O	L4	200	N3	54	59
GND	-	158	-	-	-	I/O (D1)	V3	173	U6	86	748	I/O (CS1, A2)	T2	187	U3	70	14	VCC	-	201	R1	52	-
I/O (D2)	V7	159	W8	103	709	I/O (RCLK-BUSY/RDY)	V2	174	V5	85	751	I/O (A3)	N3	188	V1	69	17	I/O	-	-	M5	51	62
I/O	U7	160	X7	102	712	I/O	-	-	W4	84	754	I/O	-	-	R4	68	20	I/O	-	-	P1	50	65
VCC	-	161	X5	-	-	I/O	-	-	W3	83	757	I/O	-	-	P5	67	23	I/O	-	-	M4	49	68
I/O	V6	162	V8	99	715	I/O	U4	175	T6	82	760	I/O	P4	189	U2	66	26	I/O	-	-	N2	48	71
I/O	U6	163	W7	98	718	I/O	T5	176	U5	81	763	I/O	N4	190	T3	65	29	I/O (A4)	M2	202	N1	47	74
I/O	R8	164	U8	97	721	I/O (D0, DIN)	U3	177	V4	80	766	I/O	P2	191	U1	64	32	I/O (A5)	M3	203	M3	46	77
I/O	R7	165	W6	96	724	SGCK4 (DOUT, I/O)	T4	178	X1	79	769	I/O	T1	192	P4	63	35	GND	-	204	-	-	-
GND	T7	166	X6	95	-	CCLK	V1	179	V3	78	-	I/O	R1	193	R3	62	38	I/O	L3	205	M2	45	80
I/O	-	-	T8	94	727	GND	-	-	T5	-	-	I/O	N2	194	N5	61	41	I/O	L2	206	L5	44	83
I/O	-	-	V7	93	730	VCC	R4	180	W1	77	-	I/O	-	195	T2	60	44	I/O	L1	207	M1	43	86
I/O	R6	167	X4	92	733	TDO	U2	181	U4	76		I/O	-	-	R2	59	47	I/O	K1	208	L4	42	89
I/O	R5	168	U7	91	736	GND	R3	182	X2	75	-	GND	M3	196	T1	58	-	I/O (A6)	K2	209	L3	41	92
I/O	V5	169	W5	90	739	I/O (A0, WS)	T3	183	W2	74	2	I/O	P1	197	N4	57	50	I/O (A7)	K3	210	L2	40	95
I/O	V4	170	V6	89	742	PGCK4 (I/O, A1)	U1	184	V2	73	5	I/O	N1	198	P3	56	53	GND	K4	211	L1	39	-
I/O	U5	171	T7	88	-	I/O	P3	185	R5	72	8	I/O	M4	199	P2	55	56						

For a detailed description of the device architecture, see pages 2-9 through 2-31.
For a detailed description of the configuration modes and their timing, see pages 2-32 through 2-55.
For detailed lists of package pinouts, see pages 2-57 through 2-67.
For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		84	100			120	144	156	160	164	191	196	208		223	225	240		299	304
TYPE		PLAST. PLCC	PLAST. PQFP	PLAST. VQFP	TOP BRAZED CQFP	CERAM PGA	PLAST. TQFP	CERAM PGA	PLAST. PQFP	TOP BRAZED CQFP	CERAM PGA	TOP BRAZED CQFP	PLAST. PQFP	METAL PQFP	CERAM. PGA	PLAST. BGA	PLAST. PQFP	METAL PQFP	CERAM. PGA	CERAM. PGA
CODE		PC84	PQ100	VQ100	CB100	PG120	TQ144	PG156	PQ160	CB164	PG191	CB196	PQ208	MQ208	PG223	BG225	PQ240	MQ240	PG299	HQ304
XC4003	-6	C I	C I			C I														
	-5	C	C			C														
	-4	C	C			C														
XC4005	-10							M B		M B										
	-6	C I	C I					C I M B	C I	M B			C I							
	-5	C I	C I					C I	C I				C I							
	-4	C	C					C	C				C							
XC4006	-6	C I						C I	C I				C I							
	-5	C I						C I	C I				C I							
	-4	C						C	C				C							
XC4008	-6	C I							C I		C I		C I	C I						
	-5	C I							C I		C		C I	C I						
	-4	C							C		C		C	C						
XC4010	-10										M B	M B								
	-6	C I							C I		C I M B	M B	C I	C I		C I				
	-5	C I							C I		C I		C I	C I		C I				
	-4	C							C		C		C	C		C				
XC4010D	-6	C I							C I				C I			C I				
	-5	C I							C I				C I			C I				
	-4	C							C				C			C				
XC4013	-6								C I				C I	C I	C I (M B)	C I	C I	C I		
	-5								C I				C I	C I	C I	C I	C I	C I		
	-4								C				C	C	C	C	C	C		
XC4013D	-6								C I				C I			C I	C I			
	-5								C I				C I			C I	C I			
	-4								C				C			C	C			
XC4020	-6												(C I)		(C I)		(C I)		(C I)	
	-5												(C I)		(C I)		(C I)		(C I)	
	-4												(C)		(C)		(C)		(C)	
XC4025	-6														C I			C I	C I	C
	-5														C I			C I	C I	C
	-4														C			C	C	C

C = Commercial = 0° to +85° C I = Industrial = -40° to +100° C M = Mil Temp = -55° to +125° C
B = MIL-STD-883C Class B Parentheses indicates future product plans

XC4010D, XC4013D Logic Cell Array

Product Specifications

Features

- Third Generation Field-Programmable Gate Array
  - Abundant flip-flops
  - Flexible function generators
  - No on-chip RAM
  - Dedicated high-speed carry-propagation circuit
  - Wide edge decoders (four per edge)
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution network
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and Interconnect
  - Low power consumption
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary-scan logic support
  - Programmable output slew rate (2 modes)
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per output
  - 24-mA sink current per output pair
- Configured by Loading Binary File
  - Unlimited reprogrammability
  - Six programming modes
- XACT Development System runs on '386/'486-type PC, Apollo, Sun-4, and Hewlett-Packard 700 series
  - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The Xc4010D and XC4013D are RAM-less, lower-cost versions of the XC4010 and XC4013. They are identical to the XC4010 and XC4013 in all respects, except for the missing on-chip RAM.

The XC4010D and XC4013D are available in most of the same PLCC, PQFP, and PGA packages as their corresponding XC4000 non-D equivalents. See page 2-70 for details.

The XC4010D and XC4013D are also pin-compatible with the XC5210 (see XC5200 Data Sheet for additional information). The XC5210 provides another possible cost-reduction path for lower-performance applications that do not use the XC4000D features like wide-decoders and carry logic.

For complete electrical specifications, see pages 2-47 through 2-55.

For a detailed description of the device features, architecture and configuration methods, see pages 2-9 through 2-45.

For a detailed list of package printouts, please use the cross-referance on page 2-70.

For package physical dimensions and thermal data, see Section 4.

Table 1. The XC4000D Family of Field-Programmable Gate Arrays

Device	XC4010/10D	XC4013/13D
Approximate Gate Count	10,000	13,000
CLB Matrix	20 x 20	24 x 24
Number of CLBs	400	576
Number of Flip-Flops	1,120	1,536
Max Decode Inputs (per side)	60	72
Max RAM Bits	12,800*	18,432*
Number of IOBs	160	192

*XC4010D and XC4013D have no RAM

XC4010D Pinouts

XC4000D Pinout Cross-Reference

Package	XC4010	XC4010D	XC4013	XC4013D	XC5210	Pinout page
84-pin PLCC	✓	✓			✓	PC84 on page 2-62
160-pin PQFP	✓	✓	✓	✓	✓	PQ160 on page 2-62
191-pin PGA	✓					PG191 on page 2-62
208-pin PQFP	✓	✓	✓	✓	✓	PQ208 on page 2-62
223-pin PGA			✓		✓	PG223 on page 2-64
225-pin BGA	✓	✓	✓	✓		BG225 on page 2-64
240-pin PQFP			✓	✓	✓	PQ240 on page 2-64

For additional information on the XC5210, please see the **XC5200 Product Description.** X6100

XC4000A
Logic Cell Array Family

Product Specifications

Features

- Third Generation Field-Programmable Gate Arrays
  - Abundant flip-flops
  - Flexible function generators
  - On-chip ultra-fast RAM
  - Dedicated high-speed carry-propagation circuit
  - Wide edge decoders (two per edge)
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution network
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and Interconnect
  - Low power consumption
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary-scan logic support
  - Programmable output slew rate (4 modes)
  - Programmable input pull-up or pull-down resistors
  - 24-mA sink current per output (48 per pair)
- Configured by Loading Binary File
  - Unlimited reprogrammability
  - Six programming modes
- XACT Development System runs on '386/'486-type PC, NEC PC, Apollo, Sun-4, and Hewlett-Packard 700 Series
  - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The XC4000A family of FPGAs offers four devices at the low end of the XC4000 family complexity range. XC4000A differs from XC4000 in four areas: fewer routing resources, fewer wide-edge decoders, higher output sink current, and improved output slew-rate control.

- The XC4000 routing structure is optimized for smaller designs, naturally requiring fewer routing resources. The XC4000A devices have four Longlines and four single-length lines per row and column, while the XC4000 devices have six Longlines and eight single-length lines per row and column. This results in a smaller chip area and lower cost per device.
- XC4000A has two wide-edge decoders on every device edge, while the XC4000 has four. All other wide-decoder features are identical in XC4000 and XC4000A.
- XC4000A outputs are specified at 24 mA, sink current, while XC4000 outputs are specified at 12 mA. The source current is the same 4 mA for both families.
- The XC4000A family offers a more sophisticated output slew-rate control structure with four configurable options for each individual output driver: fast, medium fast, medium slow, and slow. Slew-rate control can alleviate ground-bounce problems when multiple outputs switch simultaneously, and it can reduce or eliminate crosstalk and transmission-line effects on printed circuit boards.

Note that the XC4003 and XC4005 devices are available in both flavors, the lower-priced XC4003A/XC4005A with reduced routing, and the higher-priced XC4003/XC4005 with more abundant routing resources. The XC4000A devices are intended for less demanding and more structured designs, and the XC4000 devices for more random designs requiring additional routing resources.

The equivalent devices are pin-compatible and are available in identical packages, but they are not bitstream compatible. In order to move from a XC4000A to a XC4000, or vice versa, the design must be recompiled.

Table 1. The XC4000A Family of Field-Programmable Gate Arrays

Device	XC4002A	XC4003A	XC4004A	XC4005A
Appr. Gate Count	2,000	3,000	4,000	5,000
CLB Matrix	8 x 8	10 x 10	12 x 12	14 x 14
Number of CLBs	64	100	144	196
Number of Flip-Flops	256	360	480	616
Max Decode Inputs (per side)	24	30	36	42
Max RAM Bits	2,048	3,200	4,608	6,272
Number of IOBs	64	80	96	112

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+ 260	°C
T_J	Junction temperature	+ 150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to 100°C junction	4.5	5.5	V
	Supply voltage relative to GND Military –55°C to 125°C case	4.5	5.5	V
V_{IH}	High-level input voltage (XC4000 has TTL-like input thresholds)	2.0	Vcc	V
V_{IL}	Low-level input voltage (XC4000 has TTL-like input thresholds)	0	0.8	V
T_{IN}	Input signal transition time		250	ns

At junction temperatures above those listed as Operating conditions, all delay parameters increase by 0.35% per °C.

DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 24 mA, V_{CC} min (Note 1)		0.4	V
I_{CCO}	Quiescent LCA supply current (Note 2)		10	mA
I_{IL}	Leakage current	–10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.25	mA
I_{RLL}	Horizontal Long Line pull-up (when selected) @ logic Low	0.2	2.5	mA

Note: 1. With 50% of the outputs simultaneously sinking 24 mA.
2. With no output current loads, no active input or longline pull-up resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, there derived from benchmark timing patterns. The following guidelines relflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade			-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4002A	8.5	7.5		ns
		XC4003A	9.0	8.0	5.0	ns
		XC4004A	9.5	8.5		ns
		XC4005A	10.0	9.0	6.0	ns
Full length, both pull-ups inputs from internal logic	T_{WAFL}	XC4002A	11.5	10.5		ns
		XC4003A	12.0	11.0	7.0	ns
		XC4004A	12.5	11.5		ns
		XC4005A	13.0	12.0	8.0	ns
Half length, one pull-up inputs from IOB I-pins	T_{WAO}	XC4002A	8.5	7.5		ns
		XC4003A	9.0	8.0	6.0	ns
		XC4004A	9.5	8.5		ns
		XC4005A	10.0	9.0	7.0	ns
Half length, one pull-up inputs from internal logic	T_{WAOL}	XC4002A	11.5	10.5		ns
		XC4003A	12.0	11.0	8.0	ns
		XC4004A	12.5	11.5		ns
		XC4005A	13.0	12.0	9.0	ns

Note: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (one of 4 modes), as listed on page 2-70.

Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade			-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
Global Signal Distribution						
From pad through **primary** buffer, to any clock k	T_{PG}	XC4002A	7.7	5.7		ns
		XC4003A	7.8	5.8	5.1	ns
		XC4004A	7.9	5.9		ns
		XC4005A	8.0	6.0	5.5	ns
From pad through **secondary** buffer, to any clock k	T_{SG}	XC4002A	8.7	6.7		ns
		XC4003A	8.8	6.8	6.3	ns
		XC4004A	8.9	6.9		ns
		XC4005A	9.0	7.0	6.7	ns

Horizontal Longline Switching Characteristic Guidelines

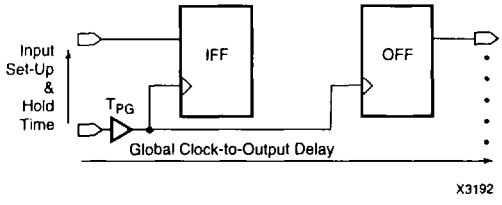
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (L.L.) I going High or Low to L.L. going High or Low, while T is Low, i.e. buffer is constantly active	T_{IO1}	XC4002A	8.2	6.0		ns
		XC4003A	8.8	6.2	4.4	ns
		XC4004A	9.4	6.6		ns
		XC4005A	10.0	7.0	5.5	ns
I going Low to L.L. going from resistive pull-up High to active Low, (TBUF configured as open drain)	T_{IO2}	XC4002A	8.7	6.5		ns
		XC4003A	9.3	6.7	5.0	ns
		XC4004A	9.9	7.1		ns
		XC4005A	10.5	7.5	6.0	ns
T going Low to L.L. going from resistive pull-up or floating High to active Low, (TUBF configured as open drain)	T_{ON}	XC4002A	10.1	8.4		ns
		XC4003A	10.7	9.0	7.2	ns
		XC4004A	11.4	9.5		ns
		XC4005A	12.0	10.0	8.0	ns
T going High to TBUF going inactive, not driving L.L.	T_{OFF}	All devices	3.0	2.0	1.8	ns
T going High to L.L. going from Low to High, pulled up by a single resistor	T_{PUS}	XC4002A	23.0	19.0		ns
		XC4003A	24.0	20.0	14.0	ns
		XC4004A	25.0	21.0		ns
		XC4005A	26.0	22.0	16.0	ns
T going High to L.L. going from Low to High, pulled up by two resistors	T_{PUF}	XC4002A	10.5	8.5		ns
		XC4003A	11.0	9.0	7.0	ns
		XC4004A	11.5	9.5		ns
		XC4005A	12.0	10.0	8.0	ns

Guaranteed Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly. and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between these two methods, the directly tested values listed below should be used, and the derived values should be ignored.

	Speed Grade		-6	-5	-4	
Description	**Symbol**	**Device**				**Units**
Global Clock to Output (fast)	T_{ICKOF}	XC4002A	14.9	12.2		ns
		XC4003A	15.1	12.5	11.6	ns
	(Max)	XC4004A	15.3	12.8		ns
		XC4005A	15.5	13.0	12.0	ns
Global Clock to Output (slew limited)	T_{ICKO}	XC4002A	19.9	15.2		ns
		XC4003A	20.1	15.5	14.6	ns
	(Max)	XC4004A	20.3	15.8		ns
		XC4005A	20.5	16.0	15.0	ns
Input Set-up Time, using IFF (no delay)	T_{PSUF}	XC4002A	2.6	2.3		ns
		XC4003A	2.4	2.0	1.6	ns
	(Min)	XC4004A	2.2	1.7		ns
		XC4005A	2.0	1.5	1.2	ns
Input Hold time, using IFF (no delay)	T_{PHF}	XC4002A	4.9	3.7		ns
		XC4003A	5.1	4.0	4.0	ns
	(Min)	XC4004A	5.3	4.3		ns
		XC4005A	5.5	4.5	4.5	ns
Input Set-up Time, using IFF (with delay)	T_{PSU}	XC4002A	21.8	18.8		ns
		XC4003A	21.5	18.5	12.0	ns
	(Min)	XC4004A	21.2	18.2		ns
		XC4005A	21.0	18.0	12.0	ns
Input Hold Time, using IFF (with delay)	T_{PH}	XC4002A	0	0		ns
		XC4003A	0	0	0	ns
	(Min)	XC4004A	0	0		ns
		XC4005A	0	0	0	ns



X3192

Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). When testing fast outputs, only one output switches. When testing slew-rate limited outputs, half the number of outputs on one side of the device are switching. These parameter values are tested and guaranteed for worst-case conditions of supply voltage and temperature, and also with the most unfavorable clock polarity choice.

T_{PDLI} for -4 Speed Grade

Pad to I1, I2 via transparent latch, with delay	XC4003A	17.6 ns
	XC4005A	17.9 ns

See page 2-76

T_{PICKD} for -4 Speed Grade

Input set-up time pad to clock (IK) with delay	XC4003A	15.6 ns
	XC4005A	15.9 ns

X6091

IOB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		-6		-5		XC4003A XC4005A -4		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
INPUT								
Propagation Delays								
Pad to I1, I2	T_{PID}		4.0		3.0		2.8	ns
Pad to I1, I2, via transparent latch (no delay)	T_{PLI}		8.0		7.0		6.0	ns
Pad to I1, I2, via transparent latch (with delay)	T_{PDLI}		26.0		24.0		**	ns
Clock (IK) tol1, I2, (flip-flop)	T_{IKRI}		8.0		7.0		6.0	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}		8.0		7.0		6.0	ns
Set-up Time (Note 3)								
Pad to Clock (IK), no delay	T_{PICK}	7.0		6.0		4.0		ns
Pad to Clock (IK) with delay	T_{PICKD}	25.0		24 .0		**		ns
Hold Time (Note 3)								
Pad to Clock (IK), no delay	T_{IKPI}	1.0		1.0		1.0		ns
Pad to Clock (IK) with delay	T_{IKPID}	neg		neg		neg		ns
OUTPUT								
Propagation Delays								
Clock (OK) to Pad (fast)	T_{OKPOF}		7.5		7.0		6.5	ns
Output (O) to Pad (fast)	T_{OPF}		9.0		7.0		5.5	ns
3-state to Pad begin hi-Z (slew-rate independent)	T_{TSHZ}		9.0		7.0		6.5	ns
3-state to Pad active and valid (fast)	T_{TSONF}		13.0		10.0		9.5	ns
Additional Delay								
For medium fast outputs			2.0		1.5		1.0	ns
For medium slow outputs			4.0		3.0		2.0	ns
For slow outputs			6.0		4.5		3.0	ns
Set-up and Hold Times								
Output (O) to clock (OK) set-up time	T_{OOK}	8.0		6.0		5.5		ns
Output (O) to clock (OK) hold time	T_{OKO}	0.0		0.0		0		ns
Clock								
Clock High or Low time	T_{CH}/T_{CL}	5.0		4.0		4.0		ns
Global Set/Reset								
Delay from GSR net through Q to I1, I2	T_{RRI}		14.5		13.5		13.5	ns
Delay from GSR net to Pad	T_{RPO}		18.0		17.0		14.6	ns
GSR width*	T_{MRW}	21.0		18.0		18.0		ns

* Timing is based on the XC4005. For other devices see XACT timing calculator.
** See preceding page.

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).

2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor or alternatively configured as a driven output or be driven from an external source.

3. Input pad setup times and hold times are specified with respect to the internal clock (IK). To calculate system setup time, subtract clock delay (clock pad to IK) from the specified input pad setup time value, but do not subtract below zero. Negative hold time means that the delay in the input data is adequate for the **external system hold time** to be zero, provided the input clock uses the Global signal distribution from pad to IK.

CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade		-6		-5		XC4003A XC4005A -4		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delays								
F/G inputs to X/Y outputs	T_{ILO}		6.0		4.5		4.0	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		8.0		7.0		6.0	ns
C inputs via H' to X/Y outputs	T_{HHO}		7.0		5.0		4.5	ns
CLB Fast Carry Logic								
Operand inputs (F1,F2,G1,G4) to C_{OUT}	T_{OPCY}		7.0		5.5		5.0	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		8.0		6.0		5.5	ns
Initialization inputs (F1,F3) to C_{OUT}	T_{INCY}		6.0		4.0		3.5	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		8.0		6.0		5.5	ns
C_{IN} to C_{OUT}, bypass function generators.	T_{BYP}		2.0		1.5		1.5	ns
Sequential Delays								
Clock K to outputs Q	T_{CKO}		5.0		3.0		3.0	ns
Set-up Time before Clock K								
F/G inputs	T_{ICK}	6.0		4.5		4.5		ns
F/G inputs via H'	T_{IHCK}	8.0		6.0		6.0		ns
C inputs via H1	T_{HHCK}	7.0		5.0		5.0		ns
C inputs via DIN	T_{DICK}	4.0		3.0		3.0		ns
C inputs via EC	T_{ECCK}	7.0		4.0		3.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	6.0		4.5		4.0		ns
C_{IN} input via F'/G'		8.0		6.0		5.5		ns
C_{IN} input via F'/G' and H'		10.0		7.5		7.3		ns
Hold Time after Clock K								
F/G inputs	T_{CKI}	0		0		0		ns
F/G inputs via H'	T_{CKIH}	0		0		0		ns
C inputs via H1	T_{CKHH}	0		0		0		ns
C inputs via DIN	T_{CKDI}	0		0		0		ns
C inputs via EC	T_{CKEC}	0		0		0		ns
C inputs via S/R, going Low (inactive)	T_{CKR}	0		0		0		ns
Clock								
Clock High time	T_{CH}	5.0		4.0		4.0		ns
Clock Low time	T_{CL}	5.0		4.0		4.0		ns
Set/Reset Direct								
Width (High)	T_{RPW}	5.0		4.0		4.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		9.0		8.0		7.0	ns
Master Set/Reset*								
Width (High or Low)	T_{MRW}	21.0		18.0		18.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}		33.0		31.0		28.0	ns

* Timing is based on the XC4005. For other devices see XACT timing calculator.

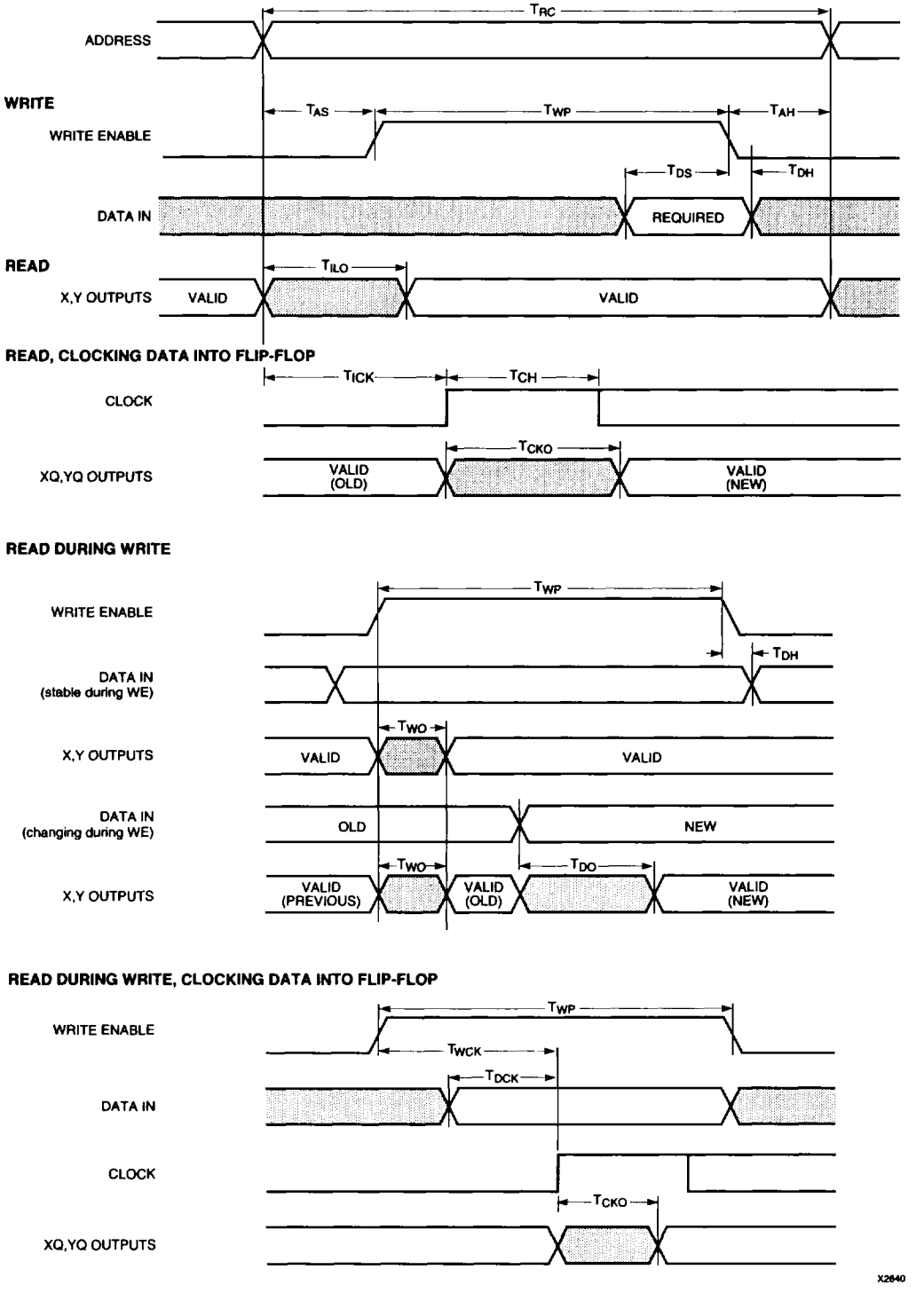
CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

CLB RAM OPTION	Speed Grade		-6		-5		XC4003A XC4005A -4		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Write Operation									
Address write cycle time	16 x 2	T_{WC}	9.0		8.0		8.0		ns
	32 x 1	T_{WCT}	9.0		8.0		8.0		ns
Write Enable pulse width (High)	16 x 2	T_{WP}	5.0		4.0		4.0		ns
	32 x 1	T_{WPT}	5.0		4.0		4.0		ns
Address set-up time before beginning of WE	16 x 2	T_{AS}	2.0		2.0		2.0		ns
	32 x 1	T_{AST}	2.0		2.0		2.0		ns
Address hold time after end of WE	16 x 2	T_{AH}	2.0		2.0		2.0		ns
	32 x 1	T_{AHT}	2.0		2.0		2.0		ns
DIN set-up time before end of WE	16 x 2	T_{DS}	4.0		4.0		4.0		ns
	32 x 1	T_{DST}	5.0		5.0		5.0		ns
DIN hold time after end of WE	both	T_{DHT}	2.0		2.0		2.0		ns
Read Operation									
Address read cycle time	16 x 2	T_{RC}	7.0		5.5		5.0		ns
	32 x 1	T_{RCT}	10.0		7.5		7.0		ns
Data valid after address change	16 x 2	T_{ILO}		6.0		4.5		4.0	ns
(no Write Enable)	32 x 1	T_{IHO}		8.0		7.0		6.0	ns
Read Operation, Clocking Data into Flip-Flop									
Address setup time before clock K	16 x 2	T_{ICK}	6.0		4.5		4.5		ns
	32 x 1	T_{IHCK}	8.0		6.0		6.0		ns
Read During Write									
Data valid after WE going active	16 x 2	T_{WO}		12.0		10.0		9.0	ns
(DIN stable before WE)	32 x 1	T_{WOT}		15.0		12.0		11.0	ns
Data valid after DIN	16 x 2	T_{DO}		11.0		9.0		8.5	ns
(DIN change during WE)	32 x 1	T_{DOT}		14.0		11.0		11.0	ns
Read During Write, Clocking Data into Flip-Flop									
WE setup time before clock K	16 x 2	T_{WCK}	12.0		10.0		9.5		ns
	32 x 1	T_{WCKT}	15.0		12.0		11.5		ns
Data setup time before clock K	16 x 2	T_{DCK}	11.0		9.0		9.0		ns
	32 x 1	T_{DCKT}	14.0		11.0		11.0		ns

Note: Timing for the 16 x 1 RAM option is identical to 16 x 2 RAM timing

CLB RAM Timing Characteristics



XC4002A Pinouts

Pin Description	PC 84	PQ100	VQ100	PG120	Bound Scan
VCC	2	92	89	G3	–
I/O (A8)	3	93	90	G1	26
I/O (A9)	4	94	91	F1	29
–	–	95*	92*	E1*	–
–	–	96*	93*	F2*	–
I/O (A10)	5	97	94	F3	32
I/O (A11)	6	98	95	D1	35
–	–	–	–	E2*	–
I/O (A12)	7	99	96	C1	38
I/O (A13)	8	100	97	D2	41
–	–	–	–	E3*	–
–	–	–	–	B1*	–
I/O (A14)	9	1	98	C2	44
SGCK1 (A15, I/O)	10	2	99	D3	47
VCC	11	3	100	C3	–
GND	12	4	1	C4	–
PGCK1 (A16, I/O)	13	5	2	B2	50
I/O (A17)	14	6	3	B3	53
–	–	–	–	A1*	–
–	–	–	–	A2*	–
I/O (TDI)	15	7	4	C5	56
I/O (TCK)	16	8	5	B4	59
–	–	–	–	A3*	–
I/O (TMS)	17	9	6	B5	62
I/O	18	10	7	A4	65
–	–	–	–	C6*	–
–	–	11*	8*	A5*	–
I/O	19	12	9	B6	68
I/O	20	13	10	A6	71
GND	21	14	11	B7	–
VCC	22	15	12	C7	–
I/O	23	16	13	A7	74
I/O	24	17	14	A8	77
–	–	18*	15*	A9*	–
–	–	–	–	B8*	–
I/O	25	19	16	C8	80
I/O	26	20	17	A10	83
I/O	27	21	18	B9	86
I/O	–	22	19	A11	89
–	–	–	–	B10*	–

Pin Description	PC 84	PQ100	VQ100	PG120	Bound Scan
I/O	28	23	20	C9	92
SGCK2 (I/O)	29	24	21	A12	95
O (M1)	30	25	22	B11	98
GND	31	26	23	C10	–
I (M0)	32	27	24	C11	101†
VCC	33	28	25	D11	–
I (M2)	34	29	26	B12	102†
PGCK2 (I/O)	35	30	27	C12	103
I/O (HDC)	36	31	28	A13	106
–	–	–	–	B13*	–
–	–	–	–	E11*	–
I/O	–	32	29	D12	109
I/O (LDC)	37	33	30	C13	112
I/O	38	34	31	E12	115
I/O	39	35	32	D13	118
–	–	36*	33*	F11*	–
–	–	37*	34*	E13*	–
I/O	40	38	35	F12	121
I/O (ERR, INIT)	41	39	36	F13	124
VCC	42	40	37	G12	–
GND	43	41	38	G11	–
I/O	44	42	39	G13	127
I/O	45	43	40	H13	130
–	–	44*	41*	J13*	–
–	–	45*	42*	H12*	–
I/O	46	46	43	H11	133
I/O	47	47	44	K13	136
I/O	48	48	45	J12	139
I/O	49	49	46	L13	142
–	–	–	–	K12*	–
–	–	–	–	J11*	–
I/O	50	50	47	M13	145
SGCK3 (I/O)	51	51	48	L12	148
GND	52	52	49	K11	–
DONE	53	53	50	L11	–
VCC	54	54	51	L10	–
PROG	55	55	52	M12	–
I/O (D7)	56	56	53	M11	151
PGCK3 (I/O)	57	57	54	N13	154
–	–	–	–	N12*	–

Pin Description	PC 84	PQ100	VQ100	PG120	Bound Scan
–	–	–	–	L9	–
I/O (D6)	58	58	55	M10	157
I/O	–	59	56	N11	160
I/O (D5)	59	60	57	M9	163
I/O ($\overline{CSO}$)	60	61	58	N10	166
–	–	62*	59*	L8*	–
–	–	63*	60*	N9*	–
I/O (D4)	61	64	61	M8	169
I/O	62	65	62	N8	172
VCC	63	66	63	M7	–
GND	64	67	64	L7	–
I/O (D3)	65	68	65	N7	175
I/O ($\overline{RS}$)	66	69	66	N6	178
–	–	70*	67*	N5*	–
–	–	–	–	M6*	–
I/O (D2)	67	71	68	L6	181
I/O	68	72	69	N4	184
I/O (D1)	69	73	70	M5	187
I/O (RCLK-$\overline{BUSY}$/RDY)	70	74	71	N3	190
–	–	–	–	M4*	–
–	–	–	–	L5*	–
I/O (D0, DIN)	71	75	72	N2	193
SGCK4 (DOUT, I/O)	72	76	73	M3	196
CCLK	73	77	74	L4	–
VCC	74	78	75	L3	–
O (TDO)	75	79	76	M2	–
GND	76	80	77	K3	–
I/O (A0, $\overline{WS}$)	77	81	78	L2	2
PGCK4 (I/O,A1)	78	82	79	N1	5
–	–	–	–	M1*	–
–	–	–	–	J3*	–
I/O (CS1, A2)	79	83	80	K2	8
I/O (A3)	80	84	81	L1	11
I/O (A4)	81	85	82	J2	14
I/O (A5)	82	86	83	K1	17
–	–	87*	84*	H3*	–
–	–	88*	85*	J1*	–
I/O (A6)	83	89	86	H2	20
I/O (A7)	84	90	87	H1	23
GND	1	91	88	G2	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 199 = BSCANT.UPD

XC4003A Pinouts

Pin Description	PC84	VQ100	PQ100	PG120	Bound Scan
VCC	2	89	92	G3	–
I/O (A8)	3	90	93	G1	32
I/O (A9)	4	91	94	F1	35
I/O	–	92	95	E1	38
I/O	–	93	96	F2	41
I/O (A10)	5	94	97	F3	44
I/O (A11)	6	95	98	D1	47
–	–	–	–	E2*	–
I/O (A12)	7	96	99	C1	50
I/O (A13)	8	97	100	D2	53
–	–	–	–	E3*	–
–	–	–	–	B1*	–
I/O (A14)	9	98	1	C2	56
SGCK1 (A15,I/O)	10	99	2	D3	59
VCC	11	100	3	C3	–
GND	12	1	4	C4	–
PGCK1 (A16, I/O)	13	2	5	B2	62
I/O (A17)	14	3	6	B3	65
–	–	–	–	A1*	–
–	–	–	–	A2*	–
I/O (TDI)	15	4	7	C5	68
I/O (TCK)	16	5	8	B4	71
–	–	–	–	A3*	–
I/O (TMS)	17	6	9	B5	74
I/O	18	7	10	A4	77
I/O	–	–	–	C6	80
I/O	–	8	11	A5	83
I/O	19	9	12	B6	86
I/O	20	10	13	A6	89
GND	21	11	14	B7	–
VCC	22	12	15	C7	–
I/O	23	13	16	A7	92
I/O	24	14	17	A8	95
I/O	–	15	18	A9	98
I/O	–	–	–	B8	101
I/O	25	16	19	C8	104
I/O	26	17	20	A10	107
I/O	27	18	21	B9	110
I/O	–	19	22	A11	113
–	–	–	–	B10*	–
I/O	28	20	23	C9	116
SGCK2 (I/O)	29	21	24	A12	119
O (M1)	30	22	25	B11	122
GND	31	23	26	C10	–
I (M0)	32	24	27	C11	125†
VCC	33	25	28	D11	–
I (M2)	34	26	29	B12	126†
PGCK2 (I/O)	35	27	30	C12	127
I/O (HDC)	36	28	31	A13	130
–	–	–	–	B13*	–
–	–	–	–	E11*	–
I/O	–	29	32	D12	133
I/O (LDC)	37	30	33	C13	136
I/O	38	31	34	E12	139
I/O	39	32	35	D13	142
I/O	–	33	36	F11	145
I/O	–	34	37	E13	148
I/O	40	35	38	F12	151
I/O (ERR, INIT)	41	36	39	F13	154
VCC	42	37	40	G12	–

Pin Description	PC84	VQ100	PQ100	PG120	Bound Scan
GND	43	38	41	G11	–
I/O	44	39	42	G13	157
I/O	45	40	43	H13	160
I/O	–	41	44	J13	163
I/O	–	42	45	H12	166
I/O	46	43	46	H11	169
I/O	47	44	47	K13	172
I/O	48	45	48	J12	175
I/O	49	46	49	L13	178
–	–	–	–	K12*	–
–	–	–	–	J11*	–
I/O	50	47	50	M13	181
SGCK3 (I/O)	51	48	51	L12	184
GND	52	49	52	K11	–
DONE	53	50	53	L11	–
VCC	54	51	54	L10	–
PROG	55	52	55	M12	–
I/O (D7)	56	53	56	M11	187
PGCK3 (I/O)	57	54	57	N13	190
–	–	–	–	N12*	–
–	–	–	–	L9*	–
I/O (D6)	58	55	58	M10	193
I/O	–	56	59	N11	196
I/O (D5)	59	57	60	M9	199
I/O ($\overline{CS0}$)	60	58	61	N10	202
I/O	–	59	62	L8	205
I/O	–	60	63	N9	208
I/O (D4)	61	61	64	M8	211
I/O	62	62	65	N8	214
VCC	63	63	66	M7	–
GND	64	64	67	L7	–
I/O (D3)	65	65	68	N7	217
I/O ($\overline{RS}$)	66	66	69	N6	220
I/O	–	67	70	N5	223
I/O	–	–	–	M6	226
I/O (D2)	67	68	71	L6	229
I/O	68	69	72	N4	232
I/O (D1)	69	70	73	M5	235
I/O (RCLK-$\overline{BUSY}$/RDY)	70	71	74	N3	238
–	–	–	–	M4*	–
–	–	–	–	L5*	–
I/O (D0, DIN)	71	72	75	N2	241
SGCK4 (DOUT, I/O)	72	73	76	M3	244
CCLK	73	74	77	L4	–
VCC	74	75	78	L3	–
O (TDO)	75	76	79	M2	–
GND	76	77	80	K3	–
I/O (A0, $\overline{WS}$)	77	78	81	L2	2
PGCK4 (A1, I/O)	78	79	82	N1	5
–	–	–	–	M1*	–
–	–	–	–	J3*	–
I/O ($\overline{CS1}$, A2)	79	80	83	K2	8
I/O (A3)	80	81	84	L1	11
I/O (A4)	81	82	85	J2	14
I/O (A5)	82	83	86	K1	17
I/O	–	84	87	H3	20
I/O	–	85	88	J1	23
I/O (A6)	83	86	89	H2	26
I/O (A7)	84	87	90	H1	29
GND	1	88	91	G2	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 247 = BSCANT.UPD

XC4004A Pinouts

Pin Description	PC84	TQ144	PQ160	PG120	Bound Scan
VCC	2	128	142	G3	–
I/O (A8)	3	129	143	G1	38
I/O (A9)	4	130	144	F1	41
I/O	–	131	145	E1	44
I/O	–	132	146	F2	47
I/O (A10)	5	133	147	F3	50
I/O (A11)	6	134	148	D1	53
–	–	135*	149*	–	–
–	–	136*	150*	–	–
GND	–	137	151	E2	–
–	–	–	152*	–	–
–	–	–	153*	–	–
I/O (A12)	7	138	154	C1	56
I/O (A13)	8	139	155	D2	59
I/O	–	140	156	E3	62
I/O	–	141	157	B1	65
I/O (A14)	9	142	158	C2	68
SGCK1 (A15, I/O)	10	143	159	D3	71
VCC	11	144	160	C3	–
GND	12	1	1	C4	–
PGCK1 (A16, I/O)	13	2	2	B2	74
I/O (A17)	14	3	3	B3	77
I/O	–	4	4	A1	80
I/O	–	5	5	A2	83
I/O (TDI)	15	6	6	C5	86
I/O (TCK)	16	7	7	B4	89
–	–	–	8*	–	–
–	–	–	9*	–	–
GND	–	8	10	A3	–
–	–	9*	11*	–	–
–	–	10*	12*	–	–
I/O (TMS)	17	11	13	B5	92
I/O	18	12	14	A4	95
I/O	–	13	15	C6	98
I/O	–	14	16	A5	101
I/O	19	15	17	B6	104
I/O	20	16	18	A6	107
GND	21	17	19	B7	–
VCC	22	18	20	C7	–
I/O	23	19	21	A7	110
I/O	24	20	22	A8	113
I/O	–	21	23	A9	116
I/O	–	22	24	B8	119
I/O	25	23	25	C8	122
I/O	26	24	26	A10	125
–	–	25*	27*	–	–
–	–	26*	28*	–	–
GND	–	27	29	–	–
–	–	–	30*	–	–
–	–	–	31*	–	–
I/O	27	28	32	B9	128
I/O	–	29	33	A11	131
I/O	–	30	34	B10	134
I/O	–	31	35	–	137

Pin Description	PC84	TQ144	PQ160	PG120	Bound Scan
I/O	28	32	36	C9	140
SGCK2 (I/O)	29	33	37	A12	143
O (M1)	30	34	38	B11	146
GND	31	35	39	C10	–
I (M0)	32	36	40	C11	149†
VCC	33	37	41	D11	–
I (M2)	34	38	42	B12	150†
PGCK2 (I/O)	35	39	43	C12	151
I/O (HDC)	36	40	44	A13	154
I/O	–	41	45	B13	157
I/O	–	42	46	E11	160
I/O	–	43	47	D12	163
I/O (LDC)	37	44	48	C13	166
–	–	–	49*	–	–
–	–	–	50*	–	–
GND	–	45	51	–	–
–	–	46*	52*	–	–
–	–	47*	53*	–	–
I/O	38	48	54	E12	169
I/O	39	49	55	D13	172
I/O	–	50	56	F11	175
I/O	–	51	57	E13	178
I/O	40	52	58	F12	181
I/O (ERR, INIT)	41	53	59	F13	184
VCC	42	54	60	G12	–
GND	43	55	61	G11	–
I/O	44	56	62	G13	187
I/O	45	57	63	H13	190
I/O	–	58	64	J13	193
I/O	–	59	65	H12	196
I/O	46	60	66	H11	199
I/O	47	61	67	K13	202
–	–	62*	68*	–	–
–	–	63*	69*	–	–
GND	–	64	70	–	–
–	–	–	71*	–	–
–	–	–	72*	–	
I/O	48	65	73	J12	205
I/O	49	66	74	L13	201
I/O	–	67	75	K12	211
I/O	–	68	76	J11	214
I/O	50	69	77	M13	217
SGCK3 (I/O)	51	70	78	L12	220
GND	52	71	79	K11	–
DONE	53	72	80	L11	–
VCC	54	73	81	L10	–
PROG	55	74	82	M12	–
I/O (D7)	56	75	83	M11	223
PGCK3 (I/O)	57	76	84	N13	226
I/O	-	77	85	N12	229
I/O	-	78	86	L9	232
I/O (D6)	58	79	87	M10	235
I/O	-	80	88	N11	238
-	-	-	89*	-	–

Pin Description	PC84	TQ144	PQ160	PG120	Bound Scan
–	–	–	90*	–	–
GND	–	81	91	–	–
–	–	82*	92*	–	–
–	–	83*	93*	–	–
I/O (D5)	59	84	94	M9	241
I/O (CSO)	60	85	95	N10	244
I/O	–	86	96	L8	247
I/O	–	87	97	N9	250
I/O (D4)	61	88	98	M8	253
I/O	62	89	99	N8	256
VCC	63	90	100	M7	–
GND	64	91	101	L7	–
I/O (D3)	65	92	102	N7	259
I/O (RS)	66	93	103	N6	262
I/O	–	94	104	N5	265
I/O	–	95	105	M6	268
I/O (D2)	67	96	106	L6	271
I/O	68	97	107	N4	274
–	–	98*	108*	–	–
–	–	99*	109*	–	–
GND	–	100	110	–	–
–	–	–	111*	–	–
–	–	–	112*	–	–
I/O (D1)	69	101	113	M5	277
I/O (RCLK-BUSY/RDY)	70	102	114	N3	280
I/O	–	103	115	M4	283
I/O	–	104	116	L5	286
I/O (D0, DIN)	71	105	117	N2	289
SGCK4 (DOUT, I/O)	72	106	118	M3	292
CCLK	73	107	119	L4	–
VCC	74	108	120	L3	–
O (TDO)	75	109	121	M2	–
GND	76	110	122	K3	–
I/O (A0, WS)	77	111	123	L2	2
PGCK4 (I/O,A1)	78	112	124	N1	5
I/O	–	113	125	M1	8
I/O	–	114	126	J3	11
I/O (CS1, A2)	79	115	127	K2	14
I/O (A3)	80	116	128	L1	17
–	–	117*	129*	–	–
–	–	–	130*	–	–
GND	–	118	131	–	–
–	–	119*	132*	–	–
–	–	120*	133*	–	–
I/O (A4)	81	121	134	J2	20
I/O (A5)	82	122	135	K1	23
–	–	–	136*	–	–
I/O	–	123	137	H3	26
I/O	–	124	138	J1	29
I/O (A6)	83	125	139	H2	32
I/O (A7)	84	126	140	H1	35
GND	1	127	141	G2	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 295 = BSCANT.UPD

XC4005A Pinouts

Pin Description	PC84	TQ144	PQ160	PQ208	PG156	Bound Scan
VCC	2	128	142	183	H3	–
I/O (A8)	3	129	143	184	H1	44
I/O (A9)	4	130	144	185	G1	47
I/O	–	131	145	186	G2	50
I/O	–	132	146	187	G3	53
–	–	–	–	188*	–	–
–	–	–	–	189*	–	–
I/O (A10)	5	133	147	190	F1	56
I/O (A11)	6	134	148	191	F2	59
I/O	–	135	149	192	E1	62
I/O	–	136	150	193	E2	65
GND	–	137	151	194	F3	–
–	–	–	–	195*	–	–
–	–	–	–	196*	–	–
–	–	–	152*	197*	D1*	–
–	–	–	153*	198*	D2*	–
I/O (A12)	7	138	154	199	E3	68
I/O (A13)	8	139	155	200	C1	71
–	–	–	–	–	–	–
I/O	–	140	156	201	C2	74
I/O	–	141	157	202	D3	77
I/O (A14)	9	142	158	203	B1	80
SGCK1 (A15, I/O)	10	143	159	204	B2	83
VCC	11	144	160	205	C3	–
–	–	–	–	206*	–	–
–	–	–	–	207*	–	–
–	–	–	–	208*	–	–
–	–	–	–	1*	–	–
GND	12	1	1	2	C4	–
–	–	–	–	3*	–	–
PGCK1 (A16, I/O)	13	2	2	4	B3	86
I/O (A17)	14	3	3	5	A1	89
I/O	–	4	4	6	A2	92
I/O	–	5	5	7	C5	95
–	–	–	–	–	–	–
I/O (TDI)	15	6	6	8	B4	98
I/O (TCK)	16	7	7	9	A3	101
–	–	–	8*	10*	A4*	–
–	–	–	9*	11*	–	–
–	–	–	–	12*	–	–
–	–	–	–	13*	–	–
GND	–	8	10	14	C6	–
I/O	–	9	11	15	B5	104
I/O	–	10	12	16	B6	107
I/O (TMS)	17	11	13	17	A5	110
I/O	18	12	14	18	C7	113
–	–	–	–	19*	–	–
–	–	–	–	20*	–	–
I/O	–	13	15	21	B7	116
I/O	–	14	16	22	A6	119
I/O	19	15	17	23	A7	122
I/O	20	16	18	24	A8	125
GND	21	17	19	25	C8	–
VCC	22	18	20	26	B8	–
I/O	23	19	21	27	C9	128
I/O	24	20	22	28	B9	131
I/O	–	21	23	29	A9	134
I/O	–	22	24	30	B10	137
–	–	–	–	31*	–	–
–	–	–	–	32*	–	–
I/O	25	23	25	33	C10	140
I/O	26	24	26	34	A10	143
I/O	–	25	27	35	A11	146
I/O	–	26	28	36	B11	149
GND	–	27	29	37	C11	–
–	–	–	–	38*	–	–
–	–	–	–	39*	–	–
–	–	–	30*	40*	A12*	–
–	–	–	31*	41*	–	–
I/O	27	28	32	42	B12	152
I/O	–	29	33	43	A13	155
I/O	–	30	34	44	A14	158
I/O	–	31	35	45	C12	161
–	–	–	–	–	–	–
I/O	28	32	36	46	B13	164
SGCK2 (I/O)	29	33	37	47	B14	167
O (M1)	30	34	38	48	A15	170
GND	31	35	39	49	C13	–
I (M0)	32	36	40	50	A16	173†
–	–	–	–	51*	–	–
–	–	–	–	52*	–	–
–	–	–	–	53*	–	–
–	–	–	–	54*	–	–
VCC	33	37	41	55	C14	–
I (M2)	34	38	42	56	B15	174†
PGCK2 (I/O)	35	39	43	57	B16	175
I/O (HDC)	36	40	44	58	D14	178
I/O	–	41	45	59	C15	181
–	–	–	–	–	–	–
I/O	–	42	46	60	D15	184
I/O	–	43	47	61	E14	187
I/O (LDC)	37	44	48	62	C16	190
–	–	–	49*	63*	E15*	–
–	–	–	50*	64*	D16*	–
–	–	–	–	65*	–	–
–	–	–	–	66*	–	–
GND	–	45	51	67	F14	–
I/O	–	46	52	68	F15	193
I/O	–	47	53	69	E16	196
I/O	38	48	54	70	F16	199
I/O	39	49	55	71	G14	202
–	–	–	–	72*	–	–
–	–	–	–	73*	–	–
I/O	–	50	56	74	G15	205
I/O	–	51	57	75	G16	208
I/O	40	52	58	76	H16	211
I/O (ERR, INIT)	41	53	59	77	H15	214
VCC	42	54	60	78	H14	–
GND	43	55	61	79	J14	–
I/O	44	56	62	80	J15	217
I/O	45	57	63	81	J16	220
I/O	–	58	64	82	K16	223
I/O	–	59	65	83	K15	226
–	–	–	–	84*	–	–
–	–	–	–	85*	–	–
I/O	46	60	66	86	K14	229
I/O	47	61	67	87	L16	232
I/O	–	62	68	88	M16	235
I/O	–	63	69	89	L15	238
GND	–	64	70	90	L14	–
–	–	–	–	91*	–	–
–	–	–	–	92*	–	–
–	–	–	71*	93*	N16*	–
–	–	–	72*	94*	M15*	–
I/O	48	65	73	95	P16	241
I/O	49	66	74	96	M14	244
I/O	–	67	75	97	N15	247
I/O	–	68	76	98	P15	250
I/O	50	69	77	99	N14	253
SGCK3 (I/O)	51	70	78	100	R16	256
GND	52	71	79	101	P14	–
–	–	–	–	102*	–	–
DONE	53	72	80	103	R15	–
–	–	–	–	104*	–	–
–	–	–	–	105*	–	–
VCC	54	73	81	106	P13	–
–	–	–	–	107*	–	–
PROG	55	74	82	108	R14	–
I/O (D7)	56	75	83	109	T16	259
PGCK3 (I/O)	57	76	84	110	T15	262
I/O	–	77	85	111	R13	265
–	–	–	–	–	–	–
I/O	–	78	86	112	P12	268
I/O(D6)	58	79	87	113	T14	271

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.

XC4005A Pinouts (continued)

Pin Descriptions	PC84	TQ144	PQ160	PQ208	PG156	Bound Scan
I/O	–	80	88	114	T13	274
–	–	–	89*	115*	R12*	–
–	–	–	90*	116*	T12*	–
–	–	–	–	117*	–	–
–	–	–	–	118*	–	–
GND	–	81	91	119	P11	–
I/O	–	82	92	120	R11	277
I/O	–	83	93	121	T11	280
I/O (D5)	59	84	94	122	T10	283
I/O ($\overline{CS0}$)	60	85	95	123	P10	286
–	–	–	–	124*	–	–
–	–	–	–	125*	–	–
I/O	–	86	96	126	R10	289
I/O	–	87	97	127	T9	292
I/O (D4)	61	88	98	128	R9	295
I/O	62	89	99	129	P9	298
VCC	63	90	100	130	R8	–
GND	64	91	101	131	P8	–
I/O (D3)	65	92	102	132	T8	301
I/O ($\overline{RS}$)	66	93	103	133	T7	304
I/O	–	94	104	134	T6	307
I/O	–	95	105	135	R7	310
–	–	–	–	136*	–	–
–	–	–	–	137*	–	–
I/O (D2)	67	96	106	138	P7	313
I/O	68	97	107	139	T5	316
I/O	–	98	108	140	R6	319
I/O	–	99	109	141	T4	322
GND	–	100	110	142	P6	–
–	–	–	–	143*	–	–
–	–	–	–	144*	–	–
–	–	–	111*	145*	R5*	–
–	–	–	112*	146*	–	–
I/O (D1)	69	101	113	147	T3	325
I/O (RCLK-$\overline{BUSY}$/RDY)	70	102	114	148	P5	328
I/O	–	103	115	149	R4	331
–	–	–	–	–	–	–
I/O	–	104	116	150	R3	334
I/O (D0, DIN)	71	105	117	151	P4	337
SGCK4 (DOUT, I/O)	72	106	118	152	T2	340
CCLK	73	107	119	153	R2	–
VCC	74	108	120	154	P3	–
–	–	–	–	155*	–	–
–	–	–	–	156*	–	–
–	–	–	–	157*	–	–
–	–	–	–	158*	–	–
O (TDO)	75	109	121	159	T1	–
GND	76	110	122	160	N3	–
I/O (A0, $\overline{WS}$)	77	111	123	161	R1	2
PGCK4 (A1, I/O)	78	112	124	162	P2	5
I/O	–	113	125	163	N2	8
–	–	–	–	–	–	–
I/O	–	114	126	164	M3	11
I/O (CS1, A2)	79	115	127	165	P1	14
I/O (A3)	80	116	128	166	N1	17
–	–	117*	129*	167*	M2*	–
–	–	–	130*	168*	M1*	–
–	–	–	–	169*	–	–
–	–	–	–	170*	–	–
GND	–	118	131	171	L3	–
I/O	–	119	132	172	L2	20
I/O	–	120	133	173	L1	23
I/O (A4)	81	121	134	174	K3	26
I/O (A5)	82	122	135	175	K2	29
–	–	–	–	176*	–	–
–	–	–	136*	177*	–	–
I/O	–	123	137	178	K1	32
I/O	–	124	138	179	J1	35
I/O (A6)	83	125	139	180	J2	38
I/O (A7)	84	126	140	181	J3	41
GND	1	127	141	182	H2	–

* Indicates unconnected package pins.
Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 343 = BSCANT.UPD

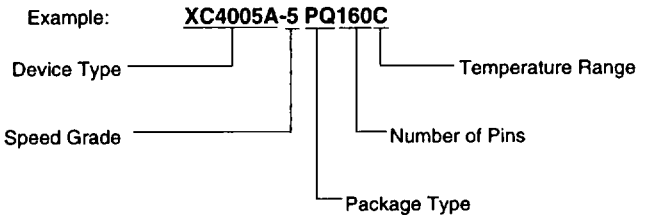
For a detailed description of the device architecture, see pages 2-9 through 2-31.

For a detailed description of the configuration modes and their timing, see pages 2-32 through 2-55.

For detailed lists of package pinouts, see pages 2-57 through 2-81 through 2-85.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		84	100			120	144	156	160	164	191	196	208		223	225	240		299
TYPE		PLAST. PLCC	PLAST. PQFP	PLAST. VQFP	TOP BRAZED CQFP	CERAM. PGA	PLAST. TQFP	CERAM PGA	PLAST. PQFP	TOP BRAZED CQFP	CERAM. PGA	TOP BRAZED CQFP	PLAST. PQFP	METAL PQFP	CERAM. PGA	PLAST. BGA	PLAST. PQFP	METAL PQFP	METAL PQFP
CODE		PC84	PQ100	VQ100	CB100	PG120	TQ144	PG156	PQ160	CB164	PG191	CB196	PQ208	MQ208	PG223	BG225	PQ240	MQ240	PG299
XC4002A	-6	C I	C I	C I		C I													
	-5	C	C	C		C													
	-4																		
XC4003A	-10				M B	M B													
	-6	C I	C I	C I	M B	C I M B													
	-5	C	C	C		C													
	-4	C	C	C		C													
XC4004A	-6	C I				C I	C I		C I										
	-5	C				C	C		C										
	-4																		
XC4005A	-6	C I					C I	C I	C I				C I						
	-5	C I					C I	C I	C I				C I						
	-4	C					C	C	C				C						

C = Commercial = 0° to +85° C I = Industrial = -40° to +100° C M = Mil Temp = -55° to +125° C
B = MIL-STD-883C Class B Parentheses indicate future product plans

XC4000H
High I/O Count
Logic Cell Array Family

Product Specifications

Features

- Third-generation Field-Programmable Gate Arrays
  - Very high number of I/O pins
  - Abundant flip-flops
  - Flexible function generators
  - On-chip ultra-fast RAM
  - Dedicated high-speed carry-propagation circuit
  - Wide edge decoders (four per edge)
  - Efficient implementation of multi-level logic
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution network
  - IEEE 1149.1-compatible boundary-scan logic support
  - Programmable output slew rate with (two modes including SoftEdge)
- Per-pin individually configurable input threshold and output high level, either TTL or CMOS
  - Programmable input pull-up or pull-down resistors
- Flexible Array Architecture
  - Programmable logic blocks and I/O blocks
  - Programmable interconnects and wide decoders
- Sub-micron CMOS Process
  - High-speed logic and interconnect
  - Low power consumption
- Configured by Loading Binary File
  - Unlimited reprogrammability
  - Six programming modes
- XACT Development System runs on '386/'486-type PC, NEC PC, Apollo, Sun-4, and Hewlett Packard 700 Series
  - Interfaces to popular design environments like Viewlogic, Mentor Graphics and OrCAD
  - Fully automatic partitioning, placement and routing
  - Interactive design editor for design optimization
  - 288 macros, 34 hard macros, RAM/ROM compiler

Description

The XC4000 family of Field-Programmable Gate Arrays (FPGAs) provides the benefits of custom CMOS VLSI, while avoiding the initial cost, time delay, and inherent risk of a conventional masked gate array.

The XC4000 family provides a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs).

Device	XC4003H	XC4005H
Approximate Gate Count	3,000	5,000
Number of IOBs	160	192
CLB Matrix	10 x 10	14 x 14
Number of CLBs	100	196
Number of Flip-Flops	200	392
Max Decode Inputs (per side)	30	42
Max RAM Bits	3,200	6,272

The XC4000H family is intended for I/O-intensive applications. Compared to the XC4000, the XC4000H devices have almost double the number of IOBs and I/O pins, and offer a choice of CMOS- or TTL-level outputs and input thresholds, selectable per pin. The XC4000H outputs sink 24 mA and offer improved 3-state and slew-rate control.

The devices are customized by loading configuration data into the internal memory cells. The FPGA can either actively read configuration data out of external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA (slave and peripheral modes).

The XC4000H family is supported by the same powerful and sophisticated software as the XC4000 family, covering every aspect of design: from schematic entry, to simulation, to automatic block placement and routing of interconnects, and finally to the creation of the configuration bit stream.

Since Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening the design and development cycle, but they also offer a cost-effective solution for production rates well beyond 1000 systems per month.

For a detailed description of the device features, architecture, configuration methods and pin descriptions, see pages 2-9 through 2-45.

XC4000H Compared to XC4000

For readers already familiar with the XC4000 family, here is a concise list of the major new features in the XC4000H family.

- Number of IOBs is, roughly, doubled compared to the XC4000.
- Output slew-rate control is significantly improved.

  Resistive Load means a strong pull-down all the way to ground, capable of sinking 24 mA continuously. If many outputs switch simultaneously, the resulting ground bounce might be objectionable.

  Capacitive Load, or SoftEdge, means a more sophisticated pull-down that decreases in strength as it approaches ground. It can only sink 4 mA at V_{OL}, which is irrelevant when driving capacitive loads. The benefit is a substantial reduction in ground bounce when several outputs switch simultaneously.

  In the XC4000, limiting the slew rate of the output reduces ground bounce, but also introduces a significant additional delay. In the XC4000H, the additional delay in the capacitive-load mode is usually insignificant.
- All input and output flip-flops have been eliminated in the XC4000H family. Use the CLB flip-flops instead.
- Outputs can sink 24 mA, guaranteed at V_{OL} = 0.5 V, compared to the 12 mA at 0.4 V of the XC4000 family.
- Number of decoder inputs per side
- Each output may be individually configured as one of the following.
  - TTL-compatible (like the XC4000) that uses n-channel transistors for both pull-down and pull-up,
  - A totem-pole output structure with reduced V_{OH},
  - CMOS-compatible (like the XC2000 and XC3000) that means n-channel pull-down and p-channel pull-up with V_{OH} close to the V_{CC} rail.
- Each input can individually be configured for either TTL-compatible threshold (1.2 V) or for CMOS-compatible threshold (V_{CC}/2). Each input can be configured to be inverting or non-inverting.
- Any combination of programmable input and output levels on any I/O pin is possible, even the dubious combination of TTL output and CMOS input on the same I/O pin.
- Output 3-state operation is controlled by a two-input multiplexer.
- The first activation of outputs after the end of the configuration process, as they change from 3-state to their active level, is always in the SoftEdge mode. This prevents potential ground-bounce problems when all outputs turn on simultaneously. A few nanoseconds later, each output assumes the current-sink capability determined by its configuration. This soft wake-up operation is transparent to the user.

Architectural Overview

Except for the I/O structure, the XC4000H family is identical to the original XC4000 family. A matrix of Configurable Logic Blocks is interconnected through a hierarchy of flexible routing resources. The powerful system-integration features of the XC4000 family, such as on-chip RAM, dedicated fast carry, and wide decoders, are retained in the XC4000H family.

The XC4000H family almost doubles the number of input/output pins compared to the XC4000, an attractive feature for I/O-intensive applications. The output drivers were redesigned to be more powerful and more flexible.

Input/Output Blocks (IOBs)

The IOBs form the interface between the internal logic and the I/O pads of the XC4000H device. Each IOB consists of a programmable output section that can drive the pad, and a programmable input section, that can receive data from the pad. Aside from being connected to the same pad, the input and output sections have nothing else in common.

Input

In XC4000H devices, there are no input flip-flops.

The input section receives data from the pad. Each input can be configured individually with TTL or CMOS input thresholds. As a configuration option, the input can be either inverted or non-inverted, before it is made available to the internal logic.

Pad

Each I/O pad can be configured with or without a pull-up or pull-down resistor, independent of the pin usage.

Boundary Scan

The XC4000H IOBs have the same IEE 1149.1boundary-scan capabilities as the IOBs in the original XC4000.

Output

In an XC4000H IOB, there is no output flip-flop. The output section receives data and 3-state control information from the CLB interconnect structure.

Under configuration control, the data can be inverted or non-inverted. The output driver assumes one of the following states.

- Permanently disabled, making the pad an input only pad
- 3-state controlled from the internal logic

There are two potential sources of the 3-state-control information, selected by a multiplexer. The output of the multiplexer driving the 3-state control can be inverted as a configuration option. The signal can be active High 3-state, which is identical to the more popular connotation of active-Low Output Enable, or it can be active-High Output Enable, which is identical to active Low 3-state.

Each output can be individually configured as either TTL- or CMOS-compatible. A TTL-compatible output uses n-channel transistors for both pull-down and pull-up. As a result, the output High voltage, V_{OH}, is at least one threshold voltage drop below V_{CC}. Depending on the load current, this means a voltage drop of 1.0 to 2.4 V. In a system using TTL input thresholds of 1.2 V, this lower output voltage results in shorter delays when switching from High to Low, and thus a better delay balance between the two signal directions. The smaller signal amplitude also generates less noise. The reduction in High-level noise margin is irrelevant because it is still much better than the Low-level noise margin. TTL-level outputs are, therefore, the best choice for systems that use TTL-level input thresholds. (XC4000 and XC4000A devices have only TTL-level outputs and have only TTL-level input thresholds).

When the output is configured as CMOS-compatible, an additional p-channel transistor pulls the output towards the V_{CC} rail. This results in an unloaded rail-to-rail signal swing, ideal for systems that use CMOS input thresholds. (XC2000 and XC3000 devices have only CMOS-level outputs).

Each output can be configured for either of two slew-rate options, which affect only the pull-down operation. When configured for resistive load, the pull-down transistor is driven hard, resulting in a practically constant on-resistance of about 10 Ω. This results in the fastest High-to-Low transition, and the capability to sink 24 mA with a voltage of 500 mV. When many outputs switch High to Low simultaneously, especially when they are discharging a capacitive load, this configuration option might result in excessive ground bounce.

When configured for capacitive load, or SoftEdge, the High-to-Low transition starts as described above, but the drive to the pull-down transistor is reduced as soon as the output voltage reaches a value around 1 V. This results in a higher resistance in the pull-down transistor, a slowing down of the falling edge, and a significantly reduced ground bounce.

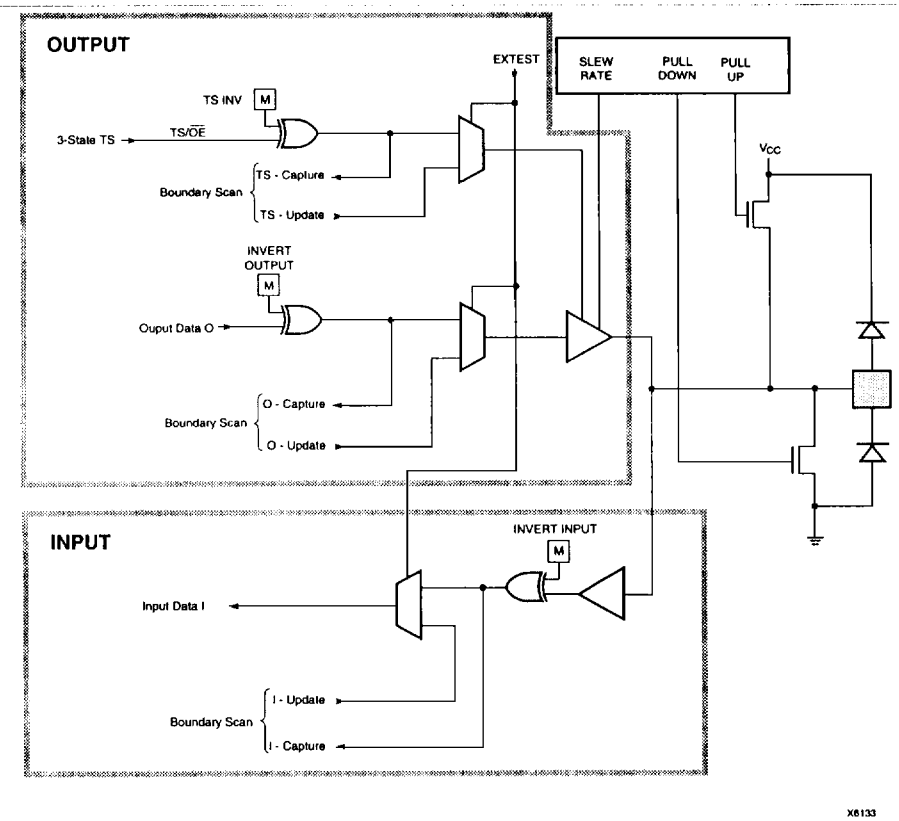


Figure 1. XC4000H Input/Output Block

Slew-Rate Control with SoftEdge

The XC4000H outputs use a novel, patent-pending method of slew-rate control that reduces ground bounce without any significant delay penalty. Each output is configured with a choice between two slew-rate options. Both options reduce the positive ground bounce that occurs when the output current is turned on. They differ in the way the output current is turned off.

- The slew-rate-limited default mode is called capacitive, or SoftEdge. At the beginning of a High-to-Low transition, the pull-down transistor is gradually turned on, and kept fully conductive until the output voltage has reached +1 V. The pull-down transistor is then gradually turned off, so that it finally has an on-resistance of about 100 Ω, low enough to sink 4 mA continuously. Gradually turning off the sink current reduces the max value of current change (di/dt) that is normally responsible for the negative voltage spike over the common ground inductance (bonding wires), called ground bounce.

  The capacitive, or SoftEdge, mode is the best choice for capacitively loaded outputs, or for outputs requiring less than 4 mA of dc sink current.

- The non-slew-rate limited mode is called resistive. At the beginning of a High-to-Low transition, the pull-down transistor is gradually turned on, and kept fully conductive as long as the output data is a logic Low. The pull-down transistor has an impedance of <20 Ω, capable of sinking 24 mA continuously.

  Resisitive mode is required for driving terminated transmission lines with 4 to 24 mA of dc sink current. The abrupt current change when the output voltage reaches zero causes a voltage spike over the ground inductance (bonding wire) and can result in objectionable ground bounce when many outputs switch High-to-Low simultaneously.

The following figures show output rising and falling edges when one output drives different loads. The tests were performed on a multi-ground-plane test PC board, manufactured by Urban Instruments (Encino, CA). Measurements were done with a Tektronix TDS540 digital storage oscilloscope. The figures below are unedited files from these measurements, the time scale is 2 ns/division.

The upper trace in each figure shows a second output driven from the same internal signal, but unloaded. It acts as a timing reference, and triggers the oscilloscope.

Resistive mode and capacitive mode transitions start with practically the same delay from the internal logic. Resisitive mode falls faster, and has more undershoot; capacitive mode rises slightly faster. For a 200-Ω pull-up, 330-Ω pull-down termination, only resisitive mode is meaningful. A TTL-output with a 1000-Ω pull-up, 150-pF termination has a slow (150 ns) final rise time that extends outside the 10-ns timing window of these figures.

Trace A shows Resistive mode with CMOS outputs
Trace B shows Resistive mode with TTL outputs
Trace C shows Capacitive mode with CMOS outputs
Trace D shows Capacitive mode with TTL outputs

Summary

Use resistive mode for applications that require >4 mA of dc sink current, and for heavy capacitive loads when they must be discharged fast. Use capacitive mode for all other applications, especially for light capacitive loads (50 to 200 pF) and for all timing-uncritical outputs that require <4 mA dc current. The Low-to-High transition is not affected by the choice of slew-rate mode.

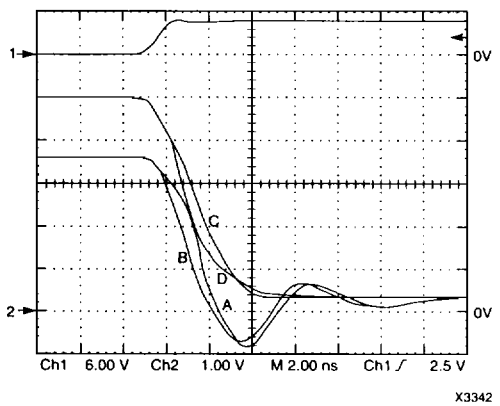


Figure 2. Falling Edge, 50 pF Load

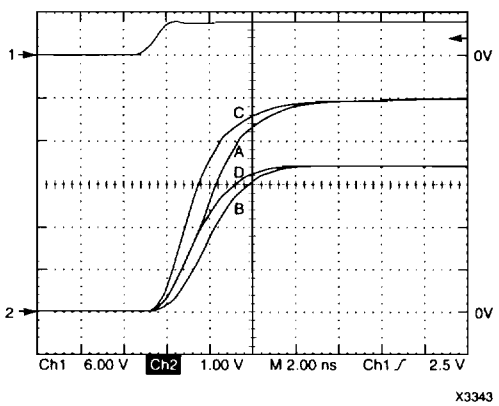


Figure 3. Rising Edge, 50 pF Load

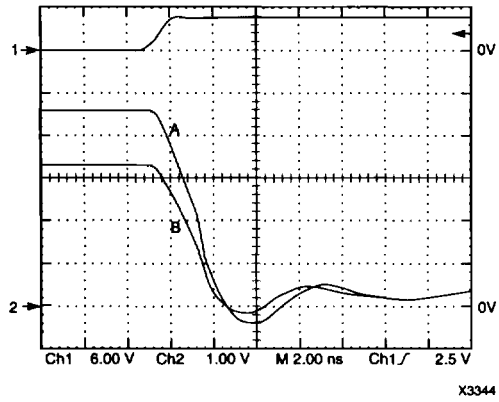


Figure 4. Falling Edge, 200/330 Ω, 50 pF Load

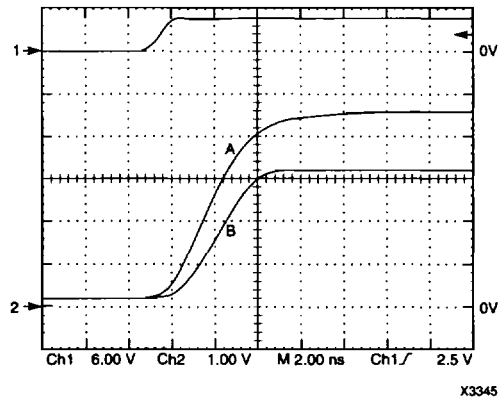


Figure 5. Rising Edge, 200/330 Ω, 50 pF Load

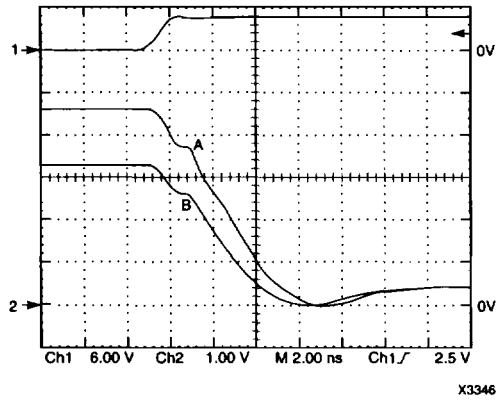


Figure 6. Falling Edge, 200/330 Ω, 150 pF Load

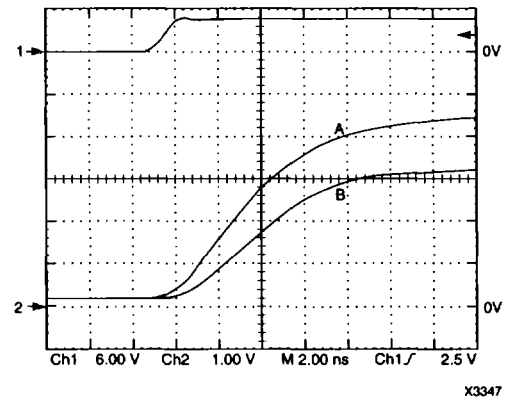


Figure 7. Rising Edge, 200/330 Ω, 150 pF Load

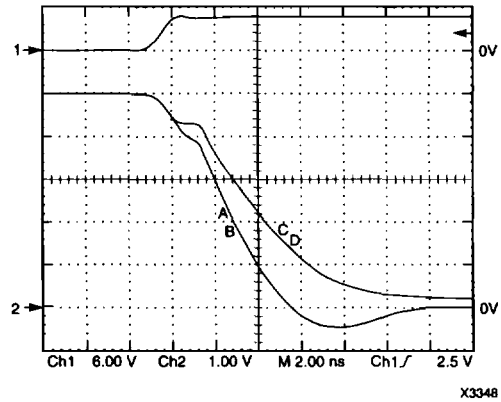


Figure 8. Falling Edge, 1000 Ω, 150 pF Load

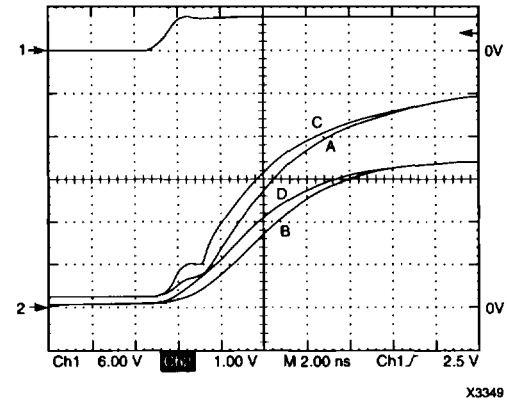


Figure 9. Rising Edge, 1000 Ω, 150 pF Load

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to + 150	°C
T_J	Junction temperature	+ 150	°C

Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial -40°C to 100°C junction	4.5	5.5	V
	Supply voltage relative to GND Military –55°C to 125°C case	4.5	5.5	V
V_{IH}	High-level input voltage for TTL threshold	2.0	V_{CC}	V
V_{IH}	High-level input voltage for CMOS threshold	70%	100%	V_{CC}
V_{IL}	Low-level input voltage for TTL threshold	0	0.8	V
V_{IL}	Low-level input voltage CMOS threshold	0	20%	V_{CC}

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.

DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage, TTL option @ I_{OH} = –4.0 mA	2.4		V
V_{OH}	High-level output voltage, CMOS option @ I_{OH} = -1 mA	V_{CC} -0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 24 mA, V_{CC} max (Note 1)		0.5	V
I_{CCO}	Quiescent LCA supply current (Note 2)		10	mA
I_{IL}	Leakage current	–10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (estimate)	0.02	0.20	mA
I_{RLL}	Horizontal Long Line pull-up (when selected) @ logic Low	0.2	2.5	mA

Note: 1. XC4003H–with 50% of the outputs simultaneously sinking 24 mA. XC4005H–with 33% of the outputs simultaneously sinking 24 mA.
2. With no output current loads, no active input or long line pull-resistors, all package pins at V_{CC} or GND, and the LCA configured with a MakeBits tie option.

Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	
Description	**Symbol**	**Device**	**Max**	**Max**	**Units**
Full length, both pull-ups, inputs from IOB i-pins	T_{WAF}	XC4003H XC4005H	9.0 10.0	8.0 9.0	ns ns
Full length, both pull-ups inputs from internal logic	T_{WAFL}	XC4003H XC4005H	12.0 13.0	11.0 12.0	ns ns
Half length, one pull-up inputs from IOB i-pins	T_{WAO}	XC4003H XC4005H	9.0 10.0	8.0 9.0	ns ns
Half length, one pull-up inputs from internal logic	T_{WAOL}	XC4003H XC4005H	12.0 13.0	11.0 12.0	ns ns

Note: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPR} or T_{OPC}), as listed on page 2-93.

Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade		-6	-5	
Description	**Symbol**	**Device**	**Max**	**Max**	**Units**
Global Signal Distribution					
From pad through **primary** buffer, to any clock k	T_{PG}	XC4003H XC4005H	7.8 8.0	5.8 6.0	ns ns
From pad through **secondary** buffer, to any clock k	T_{SG}	XC4003H XC4005H	8.8 9.0	6.8 7.0	ns ns

Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

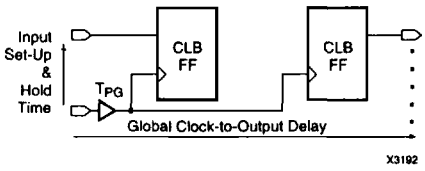
	Speed Grade		-6	-5	
Description	**Symbol**	**Device**	**Max**	**Max**	**Units**
TBUF driving a Horizontal Longline (L.L.) I going High or Low to L.L. while T is Low, i.e. buffer is constantly active	T_{IO1}	XC4003H XC4005H	8.8 10.0	6.2 7.0	ns ns
I going Low to L.L. going from resistive pull-up High to active Low, (TBUF configured as open drain)	T_{IO2}	XC4003H XC4005H	9.3 10.5	6.7 7.5	ns ns
T going Low to L.L. going from resistive pull-up or floating High to active Low, (TBUF configured as open drain)	T_{ON}	XC4003H XC4005H	10.7 12.0	9.0 10.0	ns ns
T going High to TBUF going inactive, not driving the L.L.	T_{OFF}	All devices	3.0	2.0	ns
T going High to L.L. going from Low to High, pulled up by single resistor	T_{PUS}	XC4003H XC4005H	24.0 26.0	20.0 22.0	ns ns
T going High to L.L. going from Low to High, pulled up by two resistors	T_{PUF}	XC4003H XC4005H	11.0 12.0	9.0 10.0	ns ns

Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between these two methods, the directly tested values listed below should be used, and the indirectly derived values must be ignored.

	Speed Grade		-6*	-5*	
Description	**Symbol**	**Device**			**Units**
Global Clock to Output (fast) using nearest CLB FF	T_{ICKOF} (Max)	XC4003H XC4005H			ns ns
Global Clock to Output (slew limited) using nearest CLB FF	T_{ICKO} (Max)	XC4003H XC4005H			ns ns
Input Set-up Time, using nearest CLB FF	T_{PSUF} (Min)	XC4003H XC4005H			ns ns
Input Hold time, using nearest CLB FF	T_{PHF} (Min)	XC4003H XC4005H			ns ns

* Data not available at press time



Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).

When testing fast outputs, only one output switches. When testing slew-rate limited outputs, half the number of outputs on one side of the device are switching.

These parameter values are tested and guaranteed for worst-case conditions of supply voltage and temperature, and also with the most unfavorable clock polarity choice. The use of a rising-edge clock reduces the effective clock delay by 1 to 2 ns.

The use of a rising clock edge, therefore, reduces the clock-to-output delay, and ends the hold-time requirement earlier. The use of a falling clock edge reduces the input set-up time requirement.

In the tradition of guaranteeing absolute worst-case parameter values, the table above does not take advantage of these improvements. The user can chose between a rising clock edge with slightly shorter output delay, or a falling clock edge with slightly shorter input set-up time. One of these parameters is inevitably better than the guaranteed specification listed above, albeit by only one to two nanoseconds.

CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

	Speed Grade	-6		-5		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Combinatorial Delays						
F/G inputs to X/Y outputs	T_{ILO}		6.0		4.5	ns
F/G inputs via H' to X/Y outputs	T_{IHO}		8.0		7.0	ns
C inputs via H' to X/Y outputs	T_{HHO}		7.0		5.0	ns
CLB Fast Carry Logic						
Operand inputs (F1,F2,G1,G4) to C_{OUT}	T_{OPCY}		7.0		5.5	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		8.0		6.0	ns
Initialization inputs (F1,F3) to C_{OUT}	T_{INCY}		6.0		4.0	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		8.0		6.0	ns
C_{IN} to C_{OUT}, bypass function generators.	T_{BYP}		2.0		1.5	ns
Sequential Delays						
Clock K to outputs Q	T_{CKO}		5.0		3.0	ns
Set-up Time before Clock K						
F/G inputs	T_{ICK}	6.0		4.5		ns
F/G inputs via H'	T_{IHCK}	8.0		6.0		ns
C inputs via H1	T_{HHCK}	7.0		5.0		ns
C inputs via DIN	T_{DICK}	4.0		3.0		ns
C inputs via EC	T_{ECCK}	7.0		4.0		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	6.0		4.5		ns
C_{IN} input via F'/G'		8.0		6.0		ns
C_{IN} input via F'/G' and H'		10.0		7.5		ns
Hold Time after Clock K						
F/G inputs	T_{CKI}	0		0		ns
F/G inputs via H'	T_{CKIH}	0		0		ns
C inputs via H1	T_{CKHH}	0		0		ns
C inputs via DIN	T_{CKDI}	0		0		ns
C inputs via EC	T_{CKEC}	0		0		ns
C inputs via S/R, going Low (inactive)	T_{CKR}	0		0		ns
Clock						
Clock High time	T_{CH}	5.0		4.0		ns
Clock Low time	T_{CL}	5.0		4.0		ns
Set/Reset Direct						
Width (High)	T_{RPW}	5.0		4.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		9.0		8.0	ns
Master Set/Reset*						
Width (High or Low)	T_{MRW}	21.0		18.0		ns
Delay from Global Set/Reset net to Q	T_{MRQ}		33.0		31.0	ns

* Timing is based on the XC4005H. For other devices see XACT timing calculator.

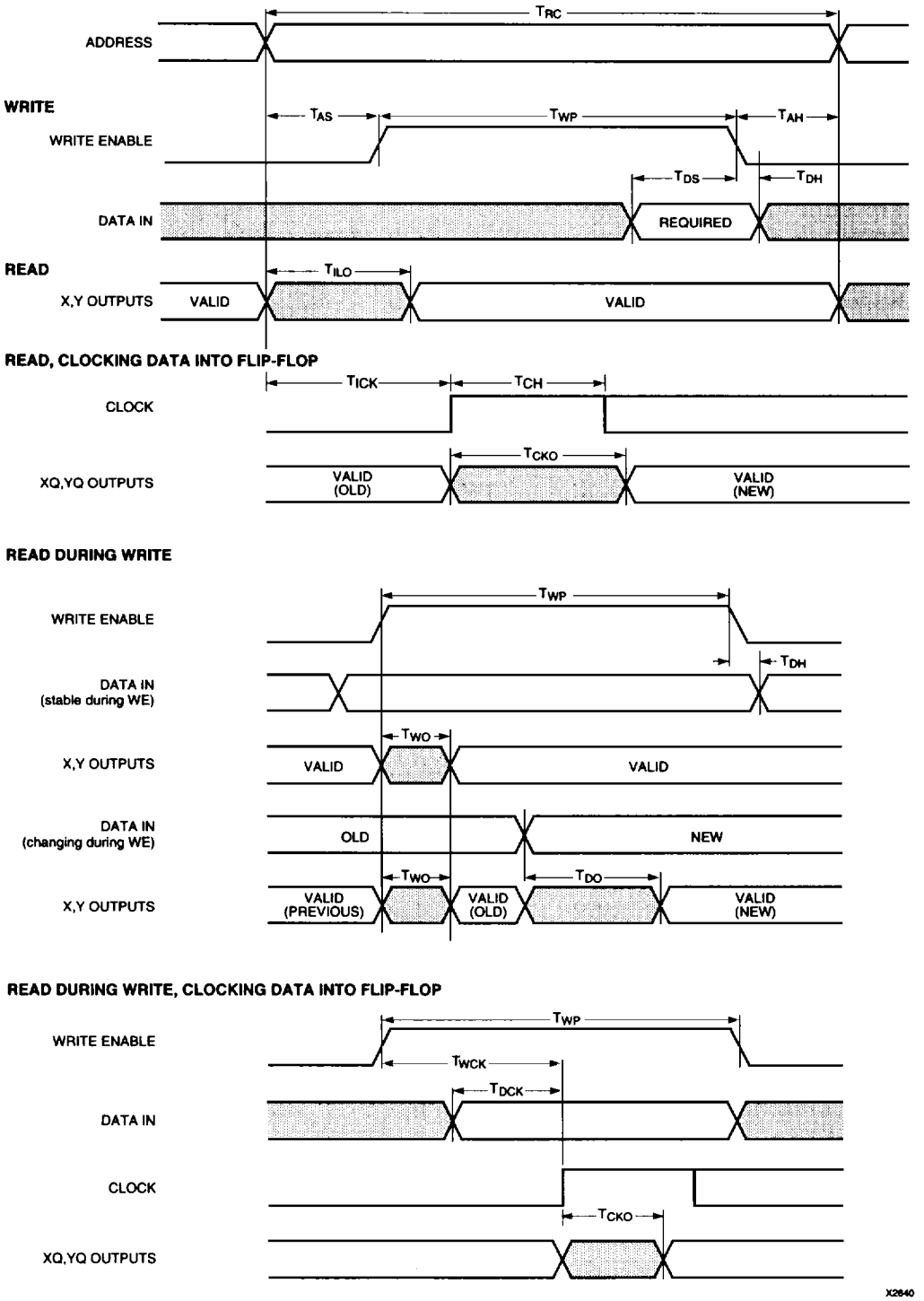
CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

CLB RAM Option	Speed Grade		-6		-5		
Description	**Symbol**		**Min**	**Max**	**Min**	**Max**	**Units**
Write Operation							
Address write cycle time	16 x 2	T_{WC}	9.0		8.0		ns
	32 x 1	T_{WCT}	9.0		8.0		ns
Write Enable pulse width (High)	16 x 2	T_{WP}	5.0		4.0		ns
	32 x 1	T_{WPT}	5.0		4.0		ns
Address set-up time before beginning of WE	16 x 2	T_{AS}	2.0		2.0		ns
	32 x 1	T_{AST}	2.0		2.0		ns
Address hold time after end of WE	16 x 2	T_{AH}	2.0		2.0		ns
	32 x 1	T_{AHT}	2.0		2.0		ns
DIN set-up time before end of WE	16 x 2	T_{DS}	4.0		4.0		ns
	32 x 1	T_{DST}	5.0		5.0		ns
DIN hold time after end of WE	both	T_{DHT}	2.0		2.0		ns
Read Operation							
Address read cycle time	16 x 2	T_{RC}	7.0		5.5		ns
	32 x 1	T_{RCT}	10.0		7.5		ns
Data valid after address change	16 x 2	T_{ILO}		6.0		4.5	ns
(no Write Enable)	32 x 1	T_{IHO}		8.0		7.0	ns
Read Operation, Clocking Data into Flip-Flop							
Address setup time before clock K	16 x 2	T_{ICK}	6.0		4.5		ns
	32 x 1	T_{IHCK}	8.0		6.0		ns
Read During Write							
Data valid after WE going active	16 x 2	T_{WO}		12.0		10.0	ns
(DIN stable before WE)	32 x 1	T_{WOT}		15.0		12.0	ns
Data valid after DIN	16 x 2	T_{DO}		11.0		9.0	ns
(DIN change during WE)	32 x 1	T_{DOT}		14.0		11.0	ns
Read During Write, Clocking Data into Flip-Flop							
WE setup time before clock K	16 x 2	T_{WCK}	12.0		10.0		ns
	32 x 1	T_{WCKT}	15.0		12.0		ns
Data setup time before clock K	16 x 2	T_{DCK}	11.0		9.0		ns
	32 x 1	T_{DCKT}	14.0		11.0		ns

Note: Timing for the 16 x 1 RAM option is identical to 16 x 2 RAM timing

CLB RAM Timing Characteristics



IOB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Inputs

Description	Symbol	-6		-5		Units
		Min	Max	Min	Max	
Propagation Delays from CMOS or TTL Levels Pad to I1, I2	T_{PID}		4.0		3.0	ns

Outputs

Description	Symbol	-6		-5		Units
		Min	Max	Min	Max	
Propagation Delays to TTL Levels						
Output (O) to Pad (Resistive Mode)	T_{OPR}		9.5		7.5	ns
Otuput (O) to Pad (Capacitive Mode)	T_{OPC}		10.5		8.0	ns
3-state to Pad begin hi-Z (Resistive Mode)	T_{TSHZR}		10.5		8.5	ns
3-state to Pad begin hi-Z (Capacitive Mode)	T_{TSHZC}		8.0		6.5	ns
3-state to Pad active and valid (Resistive Mode)	T_{TSONR}		14.0		11.0	ns
3-state to Pad active and valid (Capacitive Mode)	T_{TSONC}		16.0		12.0	ns
Propagation Delays to CMOS Levels						
Output (O) to Pad (Resistive Mode)	T_{OPR}		9.5		7.5	ns
Otuput (O) to Pad (Capacitive Mode)	T_{OPC}		9.0		7.0	ns
3-state to Pad begin hi-Z (Resistive Mode)	T_{TSHZR}		10.5		8.5	ns
3-state to Pad begin hi-Z (Capacitive Mode)	T_{TSHZC}		8.0		6.5	ns
3-state to Pad active and valid (Resistive Mode)	T_{TSONR}		14.0		11.0	ns
3-state to Pad active and valid (Capacitive Mode)	T_{TSONC}		14.0		11.0	ns

Notes: 1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture).

2. Output delays change with capacitive loading as described in the following table.

	TTL Levels	CMOS Levels	Units
Resistive Mode	0.03	0.03	ns/pF
Capacitive Mode	0.04	0.03	ns/pF

3. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up or pull-down resistor, or alternatively, configured as a driven output or be driven from an external source.

XC4003H Pinouts

Pin Description	PG191	PQ208	Bound Scan
VCC	J4	183	–
I/O (A8)	J3	184	62
I/O (A9)	J2	185	65
I/O	J1	186	68
I/O	H1	187	71
I/O	H2	188	74
I/O	H3	189	77
I/O (A10)	G1	190	80
I/O (A11)	G2	191	83
I/O	F1	192	86
I/O	E1	193	89
GND	G3	194	–
I/O	F2	195	92
I/O	D1	196	95
I/O	C1	197	98
I/O	E2	198	101
I/O (A12)	F3	199	104
I/O (A13)	D2	200	107
I/O	B1	201	110
I/O	E3	202	113
I/O (A14)	C2	203	116
SGCK1 (A15, I/O)	B2	204	119
VCC	D3	205	–
–	–	206*	–
–	–	207*	–
–	–	208*	–
–	–	1*	–
GND	D4	2	–
–	–	3*	–
PGCK1 (A16, I/O)	C3	4	122
I/O (A17)	C4	5	125
I/O	B3	6	128
I/O	C5	7	131
I/O (TDI)	A2	8	134
I/O (TCK)	B4	9	137
I/O	C6	10	140
I/O	A3	11	143
I/O	B5	12	146
I/O	B6	13	149
GND	C7	14	–
I/O	A4	15	152
I/O	A5	16	155
I/O (TMS)	B7	17	158
I/O	A6	18	161
I/O	C8	19	164
I/O	A7	20	167
I/O	B8	21	170
I/O	A8	22	173
I/O	B9	23	176
I/O	C9	24	179
GND	D9	25	–
VCC	D10	26	–

Pin Description	PG191	PQ208	Bound Scan
I/O	C10	27	182
I/O	B10	28	185
I/O	A9	29	188
I/O	A10	30	191
I/O	A11	31	194
I/O	C11	32	197
I/O	B11	33	200
I/O	A12	34	203
I/O	B12	35	206
I/O	A13	36	209
GND	C12	37	–
I/O	B13	38	212
I/O	A14	39	215
I/O	A15	40	218
I/O	C13	41	221
I/O	B14	42	224
I/O	A16	43	227
I/O	B15	44	230
I/O	C14	45	233
I/O	A17	46	236
SGCK2 (I/O)	B16	47	239
O (M1)	C15	48	242
GND	D15	49	–
I (M0)	A18	50	245†
–	–	51*	–
–	–	52*	–
–	–	53*	–
–	–	54*	–
VCC	D16	55	–
I (M2)	C16	56	246†
PGCK2 (I/O)	B17	57	247
I/O (HDC)	E16	58	250
I/O	C17	59	253
I/O	D17	60	256
I/O	B18	61	259
I/O (LDC)	E17	62	262
I/O	F16	63	265
I/O	C18	64	268
I/O	D18	65	271
I/O	F17	66	274
GND	G16	67	–
I/O	E18	68	277
I/O	F18	69	280
I/O	G17	70	283
I/O	G18	71	286
I/O	H16	72	289
I/O	H17	73	292
I/O	H18	74	295
I/O	J18	75	298
I/O	J17	76	301
I/O (ERR, INIT)	J16	77	304
VCC	J15	78	–

Pin Description	PG191	PQ208	Bound Scan
GND	K15	79	–
I/O	K16	80	307
I/O	K17	81	310
I/O	K18	82	313
I/O	L18	83	316
I/O	L17	84	319
I/O	L16	85	322
I/O	M18	86	325
I/O	M17	87	328
I/O	N18	88	331
I/O	P18	89	334
GND	M16	90	–
I/O	N17	91	337
I/O	R18	92	340
I/O	T18	93	343
I/O	P17	94	346
I/O	N16	95	349
I/O	T17	96	352
I/O	R17	97	355
I/O	P16	98	358
I/O	U18	99	361
SGCK3 (I/O)	T16	100	364
GND	R16	101	–
–	–	102*	–
DONE	U17	103	–
–	–	104*	–
–	–	105*	–
VCC	R15	106	–
–	–	107*	–
PROG	V18	108	–
I/O (D7)	T15	109	367
PGCK3 (I/O)	U16	110	370
I/O	T14	111	373
I/O	U15	112	376
I/O (D6)	V17	113	379
I/O	V16	114	382
I/O	T13	115	385
I/O	U14	116	388
I/O	V15	117	391
I/O	V14	118	394
GND	T12	119	–
I/O	U13	120	397
I/O	V13	121	400
I/O (D5)	U12	122	403
I/O (CS0)	V12	123	406
I/O	T11	124	409
I/O	U11	125	412
I/O	V11	126	415
I/O	V10	127	418
I/O (D4)	U10	128	421
I/O	T10	129	424
VCC	R10	130	–

Pin Description	PG191	PQ208	Bound Scan
GND	R9	131	–
I/O (D3)	T9	132	427
I/O (BS)	U9	133	430
I/O	V9	134	433
I/O	V8	135	436
I/O	U8	136	439
I/O	T8	137	442
I/O (D2)	V7	138	445
I/O	U7	139	448
I/O	V6	140	451
I/O	U6	141	454
GND	T7	142	–
I/O	V5	143	457
I/O	V4	144	460
I/O	U5	145	463
I/O	T6	146	466
I/O (D1)	V3	147	469
I/O (RCLK-BUSY/RDY)	V2	148	472
I/O	U4	149	475
I/O	T5	150	478
I/O (D0, DIN)	U3	151	481
SGCK4 (DOUT, I/O)	T4	152	484
CCLK	V1	153	–
VCC	R4	154	–
–	–	155*	–
–	–	156*	–
–	–	157*	–
–	–	158*	–
O (TDO)	U2	159	–
GND	R3	160	–
I/O (A0, WS)	T3	161	2
PGCK4 (I/O, A1)	U1	162	5
I/O	P3	163	8
I/O	R2	164	11
I/O (CS1, A2)	T2	165	14
I/O (A3)	N3	166	17
I/O	P2	167	20
I/O	T1	168	23
I/O	R1	169	26
I/O	N2	170	29
GND	M3	171	–
I/O	P1	172	32
I/O	N1	173	35
I/O (A4)	M2	174	38
I/O (A5)	M1	175	41
I/O	L3	176	44
I/O	L2	177	47
I/O	L1	178	50
I/O	K1	179	53
I/O (A6)	K2	180	56
I/O (A7)	K3	181	59
GND	K4	182	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 487 = BSCANT.UPD

XC4005H Pinouts

Pin Description	PG223	MQ240	Bound Scan
VCC	J4	212	–
I/O (A8)	J3	213	74
I/O (A9)	J2	214	77
I/O	J1	215	80
I/O	H1	216	83
I/O	H2	217	86
I/O	H3	218	89
GND	–	219	–
I/O (A10)	G1	220	92
I/O (A11)	G2	221	95
VCC	–	222	–
I/O	H4	223	98
I/O	G4	224	101
I/O	F1	225	104
I/O	E1	226	107
GND	G3	227	–
I/O	F2	228	110
I/O	D1	229	113
I/O	C1	230	116
I/O	E2	231	119
I/O (A12)	F3	232	122
I/O (A13)	D2	233	125
I/O	F4	234	128
I/O	E4	235	131
I/O	B1	236	134
I/O	E3	237	137
I/O (A14)	C2	238	140
SGCK1 (A15, I/O)	B2	239	143
VCC	D3	240	–
GND	D4	1	–
PGCK1 (A16,I/O)	C3	2	146
I/O (A17)	C4	3	149
I/O	B3	4	152
I/O	C5	5	155
I/O (TDI)	A2	6	158
I/O (TCK)	B4	7	161
I/O	C6	8	164
I/O	A3	9	167
I/O	B5	10	170
I/O	B6	11	173
I/O	D5	12	176
I/O	D6	13	179
GND	C7	14	–
I/O	A4	15	182
I/O	A5	16	185
I/O (TMS)	B7	17	188
I/O	A6	18	191
VCC	–	19	–
I/O	D7	20	194
I/O	D8	21	197
GND	–	22	–
I/O	C8	23	200
I/O	A7	24	203
I/O	B8	25	206
I/O	A8	26	209
I/O	B9	27	212
I/O	C9	28	215
GND	D9	29	–
VCC	D10	30	–
I/O	C10	31	218
I/O	B10	32	221
I/O	A9	33	224
I/O	A10	34	227
I/O	A11	35	230
I/O	C11	36	233
GND		37	
I/O	D11	38	236
I/O	D12	39	239
VCC	–	40	–
I/O	B11	41	242
I/O	A12	42	245
I/O	B12	43	248
I/O	A13	44	251
GND	C12	45	–
I/O	D13	46	254
I/O	D14	47	257
I/O	B13	48	260
I/O	A14	49	263
I/O	A15	50	266
I/O	C13	51	269
I/O	B14	52	272
I/O	A16	53	275
I/O	B15	54	278
I/O	C14	55	281
I/O	A17	56	284
SGCK2 (I/O)	B16	57	287
O (M1)	C15	58	290
GND	D15	59	–
I (M0)	A18	60	293†
VCC	D16	61	–
I (M2)	C16	62	294†
PGCK2 (I/O)	B17	63	295
I/O (HDC)	E16	64	298
I/O	C17	65	301
I/O	D17	66	304
I/O	B18	67	307
I/O (LDC)	E17	68	310
I/O	F16	69	313
I/O	C18	70	316
I/O	D18	71	319
I/O	F17	72	322
I/O	E15	73	325
I/O	F15	74	328
GND	G16	75	–
I/O	E18	76	331
I/O	F18	77	334
I/O	G17	78	337
I/O	G18	79	340
VCC	–	80	–
I/O	H16	81	343
I/O	H17	82	346
GND	–	83	–
I/O	G15	84	349
I/O	H15	85	352
I/O	H18	86	355
I/O	J18	87	358
I/O	J17	88	361
I/O ($\overline{ERR}$, $\overline{INIT}$)	J16	89	364
VCC	J15	90	–
GND	K15	91	–
I/O	K16	92	367
I/O	K17	93	370
I/O	K18	94	373
I/O	L18	95	376
I/O	L17	96	379
I/O	L16	97	382
GND	–	98	–
I/O	L15	99	385
I/O	M15	100	388
VCC	:	101	–
I/O	M18	102	391
I/O	M17	103	394
I/O	N18	104	397
I/O	P18	105	400
GND	M16	106	–
I/O	N15	107	403
I/O	P15	108	406
I/O	N17	109	409
I/O	R18	110	412
I/O	T18	111	415
I/O	P17	112	418
I/O	N16	113	421
I/O	T17	114	424
I/O	R17	115	427
I/O	P16	116	430
I/O	U18	117	433
SGCK3 (I/O)	T16	118	436
GND	R16	119	–
DONE	U17	120	–
VCC	R15	121	–
$\overline{PROG}$	V18	122	–
I/O (D7)	T15	123	439
PGCK3 (I/O)	U16	124	442
I/O	T14	125	445
I/O	U15	126	448
I/O	R14	127	451
I/O	R13	128	454
I/O (D6)	V17	129	457
I/O	V16	130	460
I/O	T13	131	463
I/O	U14	132	466
I/O	V15	133	469
I/O	V14	134	472
GND	T12	135	–
I/O	R12	136	475
I/O	R11	137	478
I/O	U13	138	481
I/O	V13	139	484
VCC	–	140	–
I/O (D5)	U12	141	487
I/O ($\overline{CSO}$)	V12	142	490
GND	–	143	–
I/O	T11	144	493
I/O	U11	145	496
I/O	V11	146	499
I/O	V10	147	502
I/O (D4)	U10	148	505
I/O	T10	149	508
VCC	R10	150	–
GND	R9	151	–
I/O (D3	T9	152	511
I/O ($\overline{RS}$)	U9	153	514
I/O	V9	154	517
I/O	V8	155	520
I/O	U8	156	523
I/O	T8	157	526
GND		158	
I/O (D2)	V7	159	529
I/O	U7	160	532
VCC	–	161	–
I/O	V6	162	535
I/O	U6	163	538
I/O	R8	164	541
I/O	R7	165	544
GND	T7	166	–
I/O	R6	167	547
I/O	R5	168	550
I/O	V5	169	553
I/O	V4	170	556
I/O	U5	171	559
I/O	T6	172	562
I/O (D1)	V3	173	565
I/O (RCLK-$\overline{BUSY}$/ RDY)	V2	174	568
I/O	U4	175	571
I/O	T5	176	574
I/O (D0, DIN)	U3	177	577
SGCK4 (DOUT, VO)	T4	178	580
CCLK	V1	179	–
VCC	R4	180	–
O (TDO)	U2	181	–
GND	R3	182	–
I/O (A0, $\overline{WS}$)	T3	183	2
PGCK4 (I/O, A1)	U1	184	5
I/O	P3	185	8
I/O	R2	186	11
I/O (CS1, A2)	T2	187	14
I/O (A3)	N3	188	17
I/O	P4	189	20
I/O	N4	190	23
I/O	P2	191	26
I/O	T1	192	29
I/O	R1	193	32
I/O	N2	194	35
–	–	195*	–
GND	M3	196	–
I/O	P1	197	38
I/O	N1	198	41
I/O	M4	199	44
I/O	L4	200	47
VCC	–	201	–
I/O (A4)	M2	202	50
I/O (A5)	M1	203	53
GND	–	204	–
I/O	L3	205	56
I/O	L2	206	59
I/O	L1	207	62
I/O	K1	208	65
I/O (A6)	K2	209	68
I/O (A7)	K3	210	71
GND	K4	211	–

* Indicates unconnected package pins.
† Contributes only one bit (.i) to the boundary scan register.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O

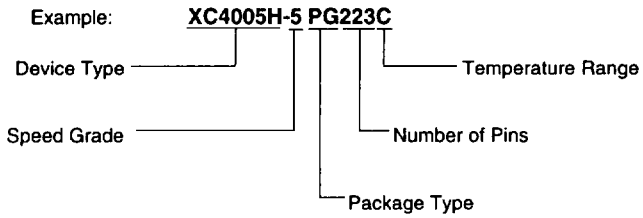
For a detailed description of the device architecture, see page 2-9 through 2-31.

For a detailed description of the configuration modes and their timing, see pages 2-32 through 2-55.

For detailed lists of package pinouts, see pages 2-100 through 2-101.

For package physical dimensions and thermal data, see Section 4.

Ordering Information



Component Availability

PINS		84	100			120	144	156	160	164	191	196	208		223	225	240		299
TYPE		PLAST. PLCC	PLAST. PQFP	PLAST. VQFP	TOP BRAZED CQFP	CERAM. PGA	PLAST. TQFP	CERAM PGA	PLAST. PQFP	TOP BRAZED CQFP	CERAM. PGA	TOP BRAZED CQFP	PLAST. PQFP	METAL PQFP	CERAM. PGA	PLAST. BGA	PLAST. PQFP	METAL PQFP	METAL PQFP
CODE		PC84	PQ100	VQ100	CB100	PG120	TQ144	PG156	PQ160	CB164	PG191	CB196	PQ208	MQ208	PG223	BG225	PQ240	MQ240	PG299
XC4003H	-6										C I		C I						
	-5										C		C						
XC4005H	-6														C I		C I	C I	
	-5														C		C	C	

C = Commercial = 0° to +85° C I = Industrial = -40° to +100° C M = Mil Temp = -55° to +125° C

B = MIL-STD-883C Class B Parentheses indicate future product plans